Suspended Gate Field Effect Transistor (SGFET)-based CMOS-MEMS Accelerometer

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Abstract

The demand for microscale sensors with integrated miniature electronic circuitry has persisted. The requirement of external amplification for the conventional MEMS accelerometer poses limitations on scaling, design, fabrication, and on-chip Integrated Circuit (IC) compatibility. These limitations could be surpassed by implementing integrated Complementary Metal Oxide Semiconductor (CMOS) - Micro-Electro-Mechanical System (MEMS) architectures for sensors. A suspended gate field effect transistor (SGFET) is a suitable candidate to be implemented as an accelerometer with in-built amplification. It obviates the need for specific interface conversion circuits compared to conventional capacitive transduction. However, specific challenges with the SGFET-based active transduction technique must be addressed to develop an SGFET-based CMOS-MEMS accelerometer for state-of-the-art devices. In this thesis, we provide solutions to the application-specific problems of the SGFET-based accelerometer, and solutions are proposed.

The first part of the thesis aimed to design, model, and simulate an SGFET-based CMOS-MEMS accelerometer by analyzing electrical and electromechanical parameters. The work involves the interaction of multiple domains, viz. mechanics, electrostatics, semiconductor physics, and circuits. A good simulation framework is essential for enabling fast sensor design optimization that helps reduce development costs. A look-up-table (LUT) approach is proposed to model and simulate the SGFET-based CMOS-MEMS accelerometer.

Secondly, the pull-in instability in the SGFET-based accelerometer limits its dynamic range and sensitivity. A novel Stepped Suspended Gate FET (SSGFET) array-based z-axis accelerometer with an enhanced detection range is proposed. The stepped gate electrode structure of SGFET aids in extending the stable driving range beyond 33.33% of the initial air-gap. The stable driving range is extended to 50% of the initial air-gap with ∼90% increase in pull-in voltage. Mechanical, electrical, and electromechanical analytical models are developed. An SSGFET-based common source (CS) amplifier with diode connected p-MOSFET load is designed and simulated in Cadence Virtuoso using the look-up table (LUT) approach. The z-axis accelerometer exhibits a sensitivity of 38 $\frac{mV}{g}$ with a supply voltage of 3.3 V for a dynamic range (DR) of $\pm$ 6 g , as compared to SGFETs with planar gate electrode which can detect up to $\pm$ 4 g with the same sensitivity.

The third part of the work focused on improving the sensitivity of the In-Plane movable SGFET (IP-SGFET) - based CMOS-MEMS accelerometer. IP-SGFET's have a suspended gate that moves in response to external input acceleration, changing the effective width of the device and, hence, the total drain current. The differential pair of fingered IP-SGFET improves the sensitivity of the IP-SGFET-based accelerometer. However, it is challenging to meet demanding high-end specifications of high sensitivity and a large measuring range, linearity, etc., without negative feedback control. Therefore, a closed-loop IP-SGFET (CLIP-SGFET) is proposed to address the abovementioned challenges. The differential amplifier's output voltage is used through a closed-loop integral control that generates a high voltage differential drive of up to 10.5±5.2 V, to drive an actuator that brings the gate back to its resting position. Appropriate design of the MEMS suspended structure, the FET device, and the interface circuit results in an open loop sensitivity of 927 mV/g with a near-zero cross-axis sensitivity with a dynamic range of ±4 g at a supply voltage of 3.3 V.

The scaling issues in SGFET are discussed in the fourth part of the work. The pseudo short channel effect (P-SCE) in SGFET at lower channel length is analyzed and quantified using key parameters like threshold voltage roll-off, drain-induced barrier lowering (DIBL), and slope of normalized output curve (α). A novel U-channel suspended gate silicon on insulator field effect transistor (USG-SOIFET) is proposed to circumvent the P-SCE in SGFET. The physical gate length (L) of USG-SOIFET is four times lower than the conventional planar channel SGFET for the same device performance. Since the same performance is achieved with a smaller length, it results in a smaller device. Investigation is carried out to scale the MEMS structure, and a four L-shaped flexure MEMS structure is used to implement a USG-SOIFET-based CMOS-MEMS accelerometer. The accelerometer's sensitivity is 4.185 μA/g with a non-linearity of 4.96% for ± 5 g detection range.

The final part of the research focused on fabricating and characterizing SGFET-based MEMS accelerometers. The unit processes were optimized, and a feasible process integration plan was developed. Devices at different stages of development are characterized to verify and optimize the device's behavior. The mechanical and electrical characterization are carried out. The accelerometer's spring constant and resonant frequency were 10.97 N/m and 7.2 kHz, respectively. The device's sensitivity was 4.72 mV/g in the ±1 g dynamic range (DR).

Keyword : Accelerometer, Active transduction technique, Complementary metal oxide semiconductor-microelectromechanical system (CMOS-MEMS), Suspended gate field effect transistor (SGFET), Look-up-table (LUT), pull-in instability, Stepped Suspended

Gate FET (SSGFET), Stable driving range, Pull-in voltage, pseudo short channel effect (P-SCE), U-channel suspended gate silicon on insulator field effect transistor (USG-SOIFET).