A Doctoral Thesis on

Resistive RAM and Neuromorphic Systems: Role of ions and interface states

(Thesis submitted in the requirements of the partial fulfilment for the degree of Doctor of Philosophy)

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ABSTRACT

This thesis uncovers the working mechanisms and the horizontal and vertical scaling limits of the most promising next-generation non-volatile memory storage scheme; that is Resistive Random Access Memory (ReRAM). By employing a Scanning tunneling microscope (STM) tip as the force electrode we were able to access the grains and grain boundaries of a Zinc Oxide switching layer and after a set of investigations, we concluded the existence of a trade-off between the scaling down and reliability of such devices below $10nm^2$ of electrode area. Next, by using the pre-established physics and mathematics (conductance vs. frequency) of a Metal-oxide-semiconductor device we understood the role of interface traps in promoting the set process of ReRAMs and the detrimental effect of these defects in sub-5nm thick devices. By using the Bias temperature stress (BTS) method and several other current-voltage measurements we recognized the ion diffusion based and oxygen vacancy based switching mechanisms in silver and gold based top electrode devices, respectively, and their subsequent effects in the technology. By depositing different thickness of Aluminium oxide (Al_2O_3) switching layer we discovered the vertical scaling being limited by different tunneling phenomena; thus restricting its lowest possible thickness to 4nm. Further, as an alternative to the conventional von Neumann computing architecture, we proposed an optical synaptic computational method with Molybdenum disulfide (MoS_2) quantum dots. We have also elucidated the nature of PPF response to different stimuli rate and their correspondence with different pass-filter responses. Finally, to evade sneak-in-leakage current in a crossbar based ReRAM organizing scheme, a combination of ReRAM and the selector device was proposed on reduced Graphene oxide (rGO) based three-terminal devices, where the set process and the off-state current was found to be a function of the applied gate voltage.