LOAD COMMUTATED CURRENT SOURCE INVERTER FED AC MOTOR DRIVES WITH OPEN-END STATOR WINDINGS

A thesis submitted
in partial fulfillment for the degree of

Doctor of Philosophy

by

RICHU SEBASTIAN C

DEPARTMENT OF AVIONICS
INDIAN INSTITUTE OF SPACE SCIENCE AND TECHNOLOGY
THIRUVANANTHAPURAM - 695547, INDIA

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To my beloved parents.

Certificate

This is to certify that the thesis entitled, **" LOAD COMMUTATED CURRENT SOURCE INVERTER FED AC MOTOR DRIVES WITH OPEN-END STATOR WINDINGS"**, submitted by **Richu Sebastian C**, to the Indian Institute of Space Science and Technology, Thiruvananthapuram, in partial fulfilment for the award of the degree of **Doctor of Philosophy**, is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Rajeevan P.P.
Research Supervisor
Associate Professor
Department of Avionics
IIST

Dr. Deepak Mishra
Associate Professor and Head
Department of Avionics
IIST

Place: Thiruvananthapuram
December 2020

Declaration

I declare that this thesis titled, **"LOAD COMMUTATED CURRENT SOURCE INVERTER FED AC MOTOR DRIVES WITH OPEN-END STATOR WINDINGS"** submitted in partial fulfilment of the degree of Doctor of Philosophy is a record of the original work carried out by me under the supervision of **Dr. RAJEEVAN P.P.,** and has not formed the basis for the award of any other degree or diploma, in this or any other Institution or University. In keeping with the ethical practice in reporting scientific information, due acknowledgements have been made wherever the findings of others have been cited.

Place: Thiruvananthapuram
December 2020

Richu Sebastian C
Department of Avionics
Roll No.: SC14D006

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RICHU SEBASTIAN C

Abstract

Silicon Controlled Rectifier (SCR) is one of the most rugged power semiconductor devices, available in high current and voltage ratings. However, being a semi-controlled device an SCR can only be turned ON by applying gate pulse but turning OFF (commutation) requires its anode current to be brought down below the holding current. Hence complex forced commutation circuits are required for SCRs, in many applications. In AC circuits, natural commutation of the SCR can be achieved if the current through the device is leading ahead of the voltage. A synchronous motor can be operated at leading power factor by resorting to over-excitation thereby making the motor current leading ahead of the voltage. This feature makes the SCR an ideal switching device in the CSI fed load commutated synchronous motor drive since the SCRs will be naturally commutated by the back-EMF of the motor (load commutation) during the inverter operation. In load commutated synchronous motor drive since the CSI is fed from a well regulated current source with a large inductor it has inherent short circuit protection. It is also free from problems like DC bus shoot through fault, encountered in VSI. These features enhance the reliability and ruggedness of load commutated synchronous motor drive. The main drawback of drive is that since large inductors are used for realizing the current source, they have slower dynamic response compared to that of VSI fed drives. However most of the medium and high power drives are used for loads like pumps, fans, conveyors and compressors where high dynamic performance is not a requirement. So, SCR based load commutated CSI fed synchronous motors are extensively used in high power drive applications.

When compared to the synchronous motors, the induction motors are more rugged, reliable, cheaper, and efficient and hence always preferred in industrial applications. However, since the induction motor operates at lagging power factor it was not possible to achieve load commutation of SCRs in load commutated induction motor drives unlike synchronous motor drives. If the load commutation can be achieved in SCR based CSI

fed induction motor drive, it would be a very good choice in many high power drive applications. In this thesis a new topology of a load-commutated silicon controlled rectifier (SCR)-based current source inverter (CSI)-fed induction motor drive with open-end stator winding is presented. The proposed topology has a SCR based CSI connected at one end of the stator windings for feeding active power to the motor and a capacitor fed IGBT based VSI is connected at the other end of the stator windings for supplying reactive power. Load commutation of the SCRs of the CSI is achieved by controlling the VSI in such a way that it over-compensates the reactive power required by the motor so that at the CSI terminals the current leads ahead of the voltage. Since the CSI current leads ahead of the CSI terminal voltage under all conditions of operation of the motor, the SCRs of the CSI are naturally commutated. The CSI supplies the entire active power required by the motor. Since the VSI supplies only the reactive power required to maintain slightly leading power factor at the CSI terminals, the power handled by the VSI is only 20-25$\%$ of that of the CSI, for high power motors. This topology is also free from problems like commutation failure at low speeds normally encountered in CSI fed high power synchronous motor drives due to insufficient back-EMF. The experimental verification of the proposed scheme is carried out on a laboratory prototype with 1.5HP induction motor having open-end stator windings. A digital signal processor (TMS320F28335) is used for implementation of the control algorithm. The proposed scheme was also experimentally verified on a 10 HP induction motor with open-end stator windings, subsequently.

However, in the proposed scheme the motor current is quasi square wave due to the 120 degree conduction mode of CSI operation, which is rich in low order harmonics. Harmonic analysis of this motor current waveform reveals that 5^{th} and 7^{th} harmonic contents are 20$\%$ and 14.35$\%$ (of fundamental) respectively, that can result in considerable 6^{th} harmonic torque pulsations. To mitigate this, a load commutated SCR based multilevel current source inverter (CSI) configuration for open-end winding induction motor is proposed to establish multilevel motor current instead of the quasi square wave current. The multilevel current waveform is realized using two isolated load commutated SCR based current source inverters connected in parallel configuration, but operated with a phase shift of 30 degrees thereby attaining significant reduction in harmonic distortion of the motor current. Harmonic analysis of this motor current waveform reveals that 5^{th}

and 7^{th} harmonic contents are reduced to 5.36% and 3.83% respectively, that results in significant reduction in torque pulsations and the losses due to harmonics. Even in the multilevel CSI configuration the VSI connected at the other end of the stator winding of open-end winding IM is used for reactive power compensation. Even when the two CSIs are operating with a phase shift of 30 degrees, load commutation of SCRs in both CSIs are achieved using the VSI. A new closed loop control scheme was developed and implemented to achieve this task. The proposed multilevel CSI fed IM drive scheme is experimentally verified on an induction motor with open-end stator winding.

A major problem faced in the conventional load commutated current source inverter fed synchronous motor drive is the commutation failure during low speed operation due to insufficient back-EMF. The scheme adopted by the industry as a solution for this problem is to employ pulsed mode of operation during starting and at low speed. However, the pulsed mode of operation results in undesirable high torque pulsation. A new scheme to facilitate hassle-free load commutation of CSI fed synchronous motor drives during starting as well as at low speed without resorting to pulsed mode operation is proposed in this thesis. The proposed scheme consists of an open-end winding synchronous motor with SCR based current source inverter connected to one side of the stator windings and an IGBT based voltage source inverter connected to the other side to aid commutation of SCRs when the back-EMF is insufficient. The CSI provides the real power requirement of the system, while the VSI is controlled to generate sufficient voltage which gets added to the motor back-EMF to facilitate load commutation during start-up and low speed operation. When the drive speed exceeds the change-over speed the VSI operation can be stopped and the CSI alone will be in operation. Alternatively, the VSI operation can be continued in the entire speed range if frequent operations at low speed or reversal of the speed is required.

The proposed schemes for realization of load commutated SCR based CSI fed AC motor drives have been experimentally validated under transient as well as steady state operations including speed reversal and regenerative braking.

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Abbreviations

VSI	Voltage Source Inverter
MV	Medium Voltage
SCR	Silicon Controlled Rectifier
GTO	Gate Turn-Off Thyristor
IGCT	Integrated Gate-Commutated Thyristor
MCT	MOS-Controlled Thyristor
MTO	MOS Turn-Off Thyristor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
IEGT	Injection Enhanced Gate Transistor
DTC	Direct Torque Control
VFD	Variable Frequency Drive
CSI	Current Source Inverter
LCI	Load Commutated Inverter
AFE	Active Front End Rectifier
NPC	Neutral Point Clamped Converter
ANPC	Active Neutral Point Clamped Inverter
FC	Flying-Capacitor
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
ASCI	Auto Sequential Current Source Inverter
STATCOM	Static Synchronous Compensator
ARIM	Active Reactive Induction Machine
IM	Induction Motor
EMF	Electromotive Force
DSP	Digital signal Processor
PF	Power Factor
LPF	Low Pass Filter
PI	Proportional-Integral
THD	Total Harmonic Distortion
DAC	Digital to Analog Converter
RPM	Revolutions per Minute
GPIO	General Purpose Input Output
EPWM	Enhanced Pulse Width Modulator
CPLD	Complex Programmable Logic Device
SMPS	Switched-Mode Power Supply
eQEP	Enhanced Quadrature Encoder Pulse
SCI	Serial Communication Interface

SPI	Serial Peripheral Interface
ECAN	Enhanced Controller Area Network
ADC	Analog to Digital Converter
JTAG	Joint Test Action Group

Notations

i_d	DC-link current of CSI.
i_{dref}	DC-link current reference of CSI.
v_{sa},v_{sb},v_{sc}	Instantaneous values of the CSI terminal voltages referred to fictitious neutral point.
v_{sab},v_{sbc},v_{sca}	Instantaneous values of the CSI line voltages.
i_{ma},i_{mb},i_{mc}	Instantaneous values of the motor currents in phase A, B and C.
i_{maf},i_{mbf},i_{mcf}	Instantaneous values of fundamental component of the motor currents in phase a, b and c.
v_{lab},v_{lbc}, v_{lca}	Instantaneous values of the AC supply line voltages.
V_c	VSI capacitor voltage.
V_s	CSI terminal voltage phasor.
V_v	VSI voltage phasor.
V_m	Motor voltage phasor.
V_{sd},V_{sq}	d-axis and q-axis components of the CSI terminal voltages (v_{sa}, v_{sb}, v_{sc}).
I_{mf}	Phasor representing fundamental component of the motor current.
ω_m,ω_{ref},ω_{slip}	Actual speed, reference speed, slip speed of the induction motor.
β	Angle between fundamental component of motor current and terminal voltage of the CSI.
γ	Commutation angle.
ϕ	Motor power factor angle.
v_{la},v_{lb},v_{lc}	Per-phase voltages of the AC supply.
α	Firing Angle of SCR.
t_q	turn OFF time of SCR.
i_{ga},i_{gb},i_{gc}	Unit magnitude three phase sinusoidal signals for CSI gate pulse generation.
i_m, i_{mrms}	Motor current, RMS value of the fundamental component of motor current.
V_{rec}	Current controller output of rectifier.
G_{rec}	Gain constant of the rectifier.
$i_{mf\alpha}$,$i_{mf\beta}$	α-axis and β-axis components of motor current fundamental.
$v_{s\alpha}$,$v_{s\beta}$	α-axis and β-axis components of the CSI terminal voltages.
V_{sdf},V_{sqf}	filtered d-axis and q-axis components of the CSI terminal voltages.
V_{vd},V_{vq}	d-axis and q-axis components of the VSI phase voltages.
V_{sqref}	Reference voltage to the q-axis controller .
V_{cref}	VSI Capacitor reference voltage.
$v_{v\alpha}$,$v_{v\beta}$	α-axis and β-axis components of the VSI phase voltages.
F_s	switching frequency of the VSI.
v_{vam},v_{vbm},v_{vcm}	phase A, B and C modulating signals for the VSI.
i_{ga1},i_{gb1},i_{gc1}	Unit magnitude three phase sinusoidal signals for CSI-1 gate pulse generation.
i_{ga2},i_{gb2},i_{gc2}	Unit magnitude three phase sinusoidal signals for CSI-2 gate pulse generation.
i_{d1},i_{d2}	DC-link currents of CSI-1 and CSI-2.
δ	Phase shift angle between the CSI (CSI-1 and CSI-2) operation.
I_{s1f}	Phasor representing fundamental component of the CSI-1 current.

I_{s2f}	Phasor representing fundamental component of the CSI-2 current.
a_0, a_n, b_n	Fourier series coefficients.
V_{rec-1},V_{rec-2}	Current controller output of Rectifier-1 and Rectifier-2.
α_1,α_2	SCR firing angle of Rectifier-1 and Rectifier-2.

Chapter 1

Introduction

1.1 Introduction

AC electric motors, extensively used in the industry for various applications, constitute the major load in the electrical power distribution system. Earlier they were driven by directly connecting to the power supply lines resulting in constant speed operation irrespective of the speed and torque requirements of the load. Hence the speed and the torque requirements of the loads driven by constant speed electric motors were achieved by using mechanical systems resulting in poor efficiency of the overall drive system. The increasing need for energy conservation led to the development of various types of variable speed AC drives to meet the requirements of efficient conversion of electrical energy into mechanical energy in the industry. The motor speed and torque can be varied in a wide range in variable speed AC drives driven by power electronic converters that act as interfacing equipment between the motor and the power supply lines.

Majority of the industrial drives fall in two categories; the low voltage (LV) drives (motor voltage < 2.3 kV (RMS)) and the medium voltage (MV) drives (2.3 kV to 13.8 kV). The low voltage drives are generally available in the power range from few hundred watts to few thousand watts. The medium voltage drives are used for high power applications ranging from few kilo-watts to 100 MW generally. Some manufacturers supply drives with power rating up to 150 MW in the medium voltage category. The switching frequency in medium voltage drive is often limited in the range from 500 Hz to 1 kHz. However, the majority of the installed MV drives in the industry are in the power range from 1 MW to 4 MW with voltage ratings in the range from 3.3 kV to 6.6 kV. In the medium voltage category induction motor drives and synchronous machines constitute the majority.

The development of semiconductor technology over the years has brought significant changes in the area of medium voltage drive. The selection of semiconductor devices in the drive is based on the voltage rating, current rating, switching frequency and the controllability (turn ON and turn OFF methods). Typical semiconductor devices used for medium voltage applications include thyristors like SCR, GTO, IGCT, MCT, MTO and transistor based devices like IGBT (LV-IGBT and HV-IGBT), power-MOSFET and IEGT. Figure 1.1 shows the most commonly used semiconductor devices in the power converters of medium voltage drives. Even though many new semiconductor devices have emerged recently the high power sector is still dominated by the SCRs. Recently, medium voltage SiC devices like SiC MOSFETS, SiC IGBTs have been developed but the technology is not yet matured to be considered for medium voltage drive applications. Medium voltage drives are mainly used in cement, mining, chemical, oil, gas and paper industries. They are also used in special applications like wind tunnels [1, 2, 3, 4, 5]. Generally around 80% of these drives are used in applications like fan, pump, compressor and conveyor which do not demand high dynamic response. Therefore, most of these applications do not require advanced motor control techniques like field oriented control or direct torque control, instead simple scalar control (V/f) can be used. But such industrial installations demand high reliability, as the failure of the drives can result in huge financial loss.

1.2 A brief overview of medium voltage drives

Variable speed drives employ power electronic converters to convert constant voltage constant frequency AC supply to variable voltage variable frequency AC supply. The conventional way of achieving this is to first convert AC to DC using a rectifier and then convert DC to AC of required voltage and frequency using an inverter. The inverter plays a major role in the performance of the drive as far as the quality of motor voltage and currents are concerned. Basically there are two types of inverters namely, the voltage source inverters (VSI) and the current source inverters (CSI). The intermediate energy storage element between the rectifier and the inverter will be a capacitor in the case of a VSI and that will be an inductor in the case of CSI. There are also direct AC to AC converters like cyclo-converters and matrix converters which do not use an intermediate device for

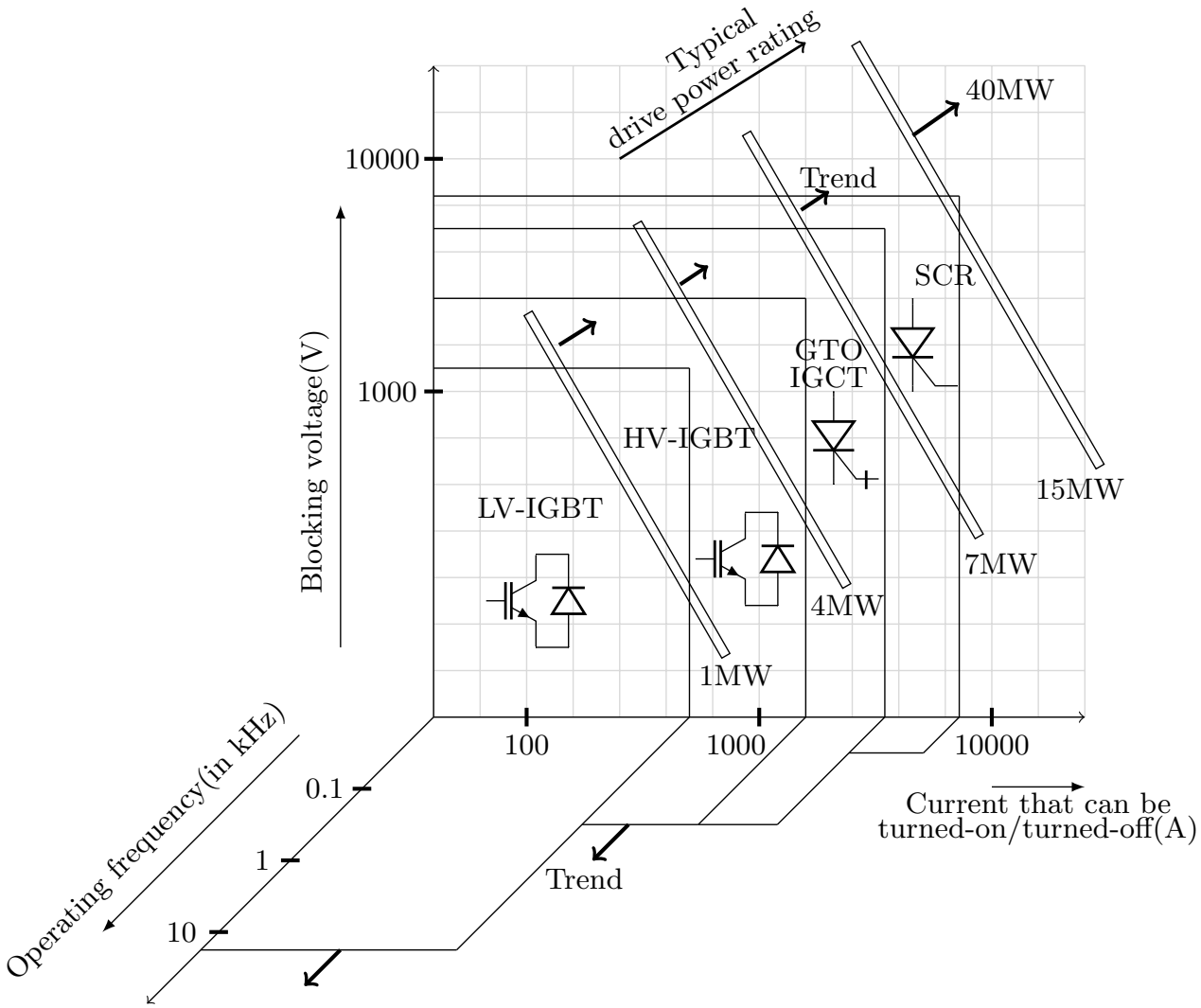

Figure 1.1: Power semiconductor devices and their ratings.

energy storage. The major types of industrial medium voltage variable speed AC motor drives are given below:

- Voltage Source Inverter (VSI) fed drives.

- Direct AC to AC converter fed drives.

- Current Source Inverter (CSI) fed drives.

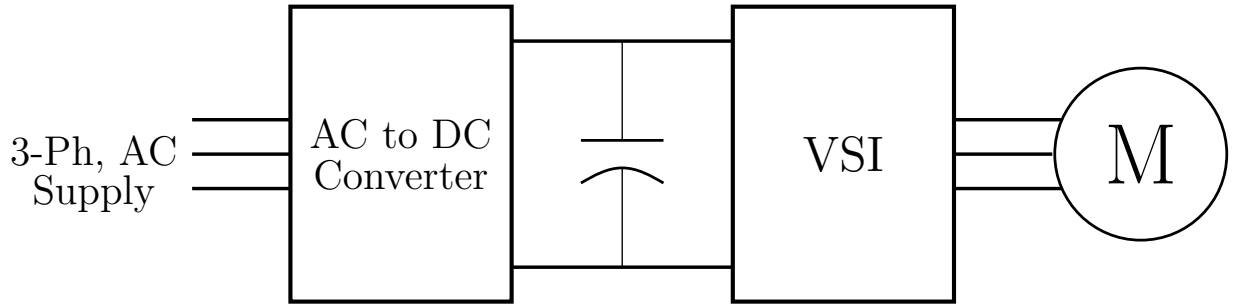

Figure 1.2: Block diagram of VSI fed drive.

1.2.1 Voltage Source Inverter fed drives

Voltage source inverter fed AC motor drives are very popular in the industry. Figure 1.2 shows the block diagram of a VSI fed AC motor drive. In most of the voltage source inverter fed drives IGBT (LV-IGBT or HV-IGBT) is used as the switching device. IGBTs are fully controlled devices which can be turned ON and OFF by using the gate. The line side AC to DC converter feeding the DC-link capacitor can either be a diode bridge rectifier or an active front end rectifier (AFE). Diode bridge rectifiers are used in most of the normal drive applications as they are very simple and cost effective. Active front end rectifier can facilitate regenerative braking and it is mainly used in applications where motor braking occurs repetitively. Since the energy stored in the inertia of the motor and the load is fed back to the utility supply lines during regenerative braking, overall efficiency of the drive system can be improved if AFE is used instead of conventional diode bridge rectifier. In addition, AFE makes the input line current almost sinusoidal and in phase with the input voltage thereby facilitating operation at almost unity power factor [6, 7].

The conventional two-level voltage source inverters are used in almost all low voltage drive applications. The multilevel voltage source inverters are generally used in medium voltage high power applications. Major advantages of using multilevel inverter configurations over the two-level inverter configuration include improved quality of output voltage waveform at reduced switching frequency, reduction in device voltage stress and reduction in electro-magnetic interference (EMI) due to low $\frac{dv}{dt}$. In addition the multilevel inverters facilitate use of low voltage devices for generation of high voltage waveforms without resorting to series connection [8, 9, 10, 11, 12, 13, 14, 15]. Conventional multi-

level inverters are neutral point clamped (NPC) inverter, flying capacitor (FC) inverter and cascaded H-bridge (CHB) inverter. A number of new multilevel inverter topologies are reported in the literature which also includes hybrid topologies formed by combining the conventional topologies. Nowadays, modular multilevel inverters have gained popularity compared to the other topologies because of its modular structure, lower cost and higher reliability. Three-level NPC inverters are also popular in the industry.

Pulse Width Modulations Schemes for VSI fed drives

The basic function of the voltage source inverters is to synthesize AC output voltage of required fundamental frequency from a constant DC voltage. Ideally the inverter connected to the motor has to create sinusoidal voltage waveform, which is often difficult to realize using power electronic switches. The quality of the output voltage created by the inverter can be greatly enhanced using pulse width modulation techniques [16, 17, 18]. Pulse-width modulation (PWM) techniques have been a topic of extensive research especially in the field of VSI fed drives [19, 20, 21, 22, 23]. Most of the pulse width modulation techniques aim to shift the harmonics in the inverter output voltage to a high frequency region so that it can be filtered out easily. In drive applications the inductance of the motor itself will act as a filter since inductive reactance will be very high at high frequencies. As a result the motor current will be almost sinusoidal even though high frequency pulsed voltage is applied to the motor. The two most popular PWM techniques are Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM).

- Sinusoidal PWM(SPWM)

  In SPWM technique several pulses of sinusoidally varying widths are created in one half cycle of the reference sine wave. This scheme basically involves comparison (using comparator) of a high frequency triangular carrier waveform (v_{car}) with sinusoidal modulating signal (v_{mod}) which represents the desired inverter output voltage as depicted in Figure 1.3. Figure 1.4 shows one leg of a three phase inverter having a high side switch (top switch) S_1 and low side switch (bottom switch) S_2. The VSI requires current bi-directional two quadrant switches which can conduct current in both directions in the ON state and block voltage of only one polarity

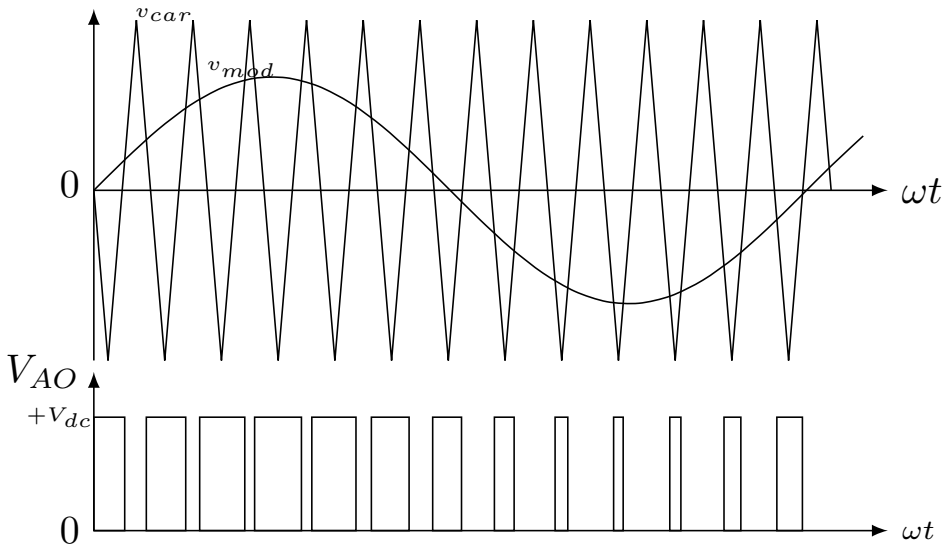

Figure 1.3: Sinusoidal PWM scheme.

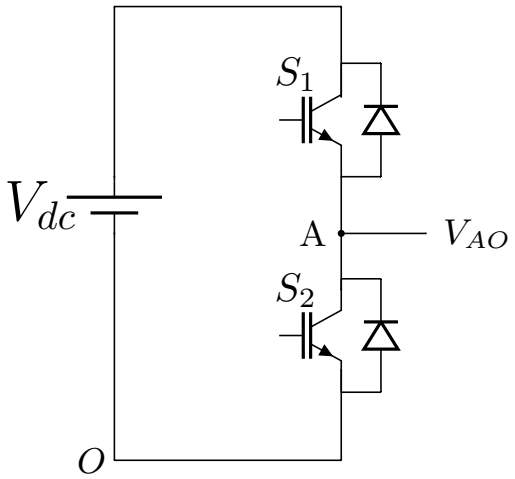

Figure 1.4: Single leg of three-phase inverter with high side switch as 'S_1' and low side switch as 'S_2'.

in the OFF state. Though the devices like power MOSFETs are used in low voltage applications, the insulated gate bipolar transistor (IGBT) is the most common switching device used in medium voltage drive applications. The voltage at the inverter pole marked 'A' with reference to the ground point 'O' is known as pole voltage (V_{AO}) of the inverter. The switches S_1 and S_2 are operated in a mutually exclusive manner. If S_1 is ON S_2 will be OFF and vice-versa. Normally a dead

band is given between the gating signals of the top switch and the bottom switch of an inverter leg so as to ensure that both switches are not turned ON simultaneously due to the difference in turn ON time and turn OFF time of the switches. Basically, the comparator output obtained by comparing v_{mod} and v_{car} is used to control the switches S_1 and S_2 of the inverter leg. When the reference signal is higher than the carrier the top switch will be turned ON, otherwise the bottom switch will be turned ON. This mode of operation results in a pulsed pole voltage (V_{AO}) with voltage levels '0' and 'V_{dc}' and the width of the pulses varies sinusoidally as shown in Figure 1.3. Harmonic analysis of this waveform will reveal that it has a fundamental frequency component having the same frequency as the reference signal and harmonic voltages in the carrier frequency region. In a three phase inverter three different modulating (sinusoidal) signals phase shifted by 120 degrees are used to compare with the same carrier wave to generate the gating signals for the switches in the three inverter legs. The frequency of the triangular carrier waveform decides the switching frequency of the inverter which is usually kept very high compared to that of the modulating signal.

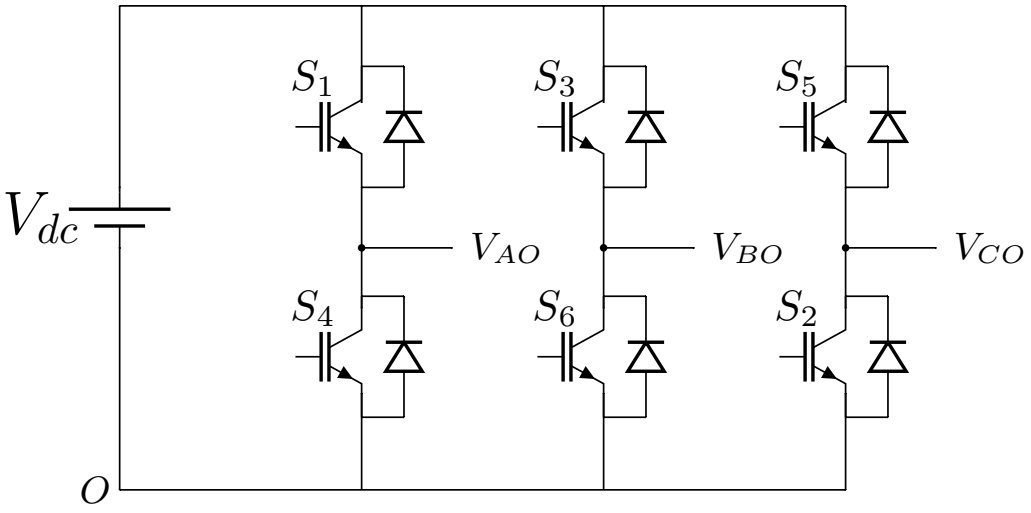

Figure 1.5: A three-phase inverter structure.

■ Space Vector PWM (SVPWM)

The concept of SVPWM has its origin in the generalized theory of AC machines. The stator windings of the AC machine, displaced in space by 120 degrees, when fed with three-phase balanced currents, phase shifted by 120 degrees, produces a

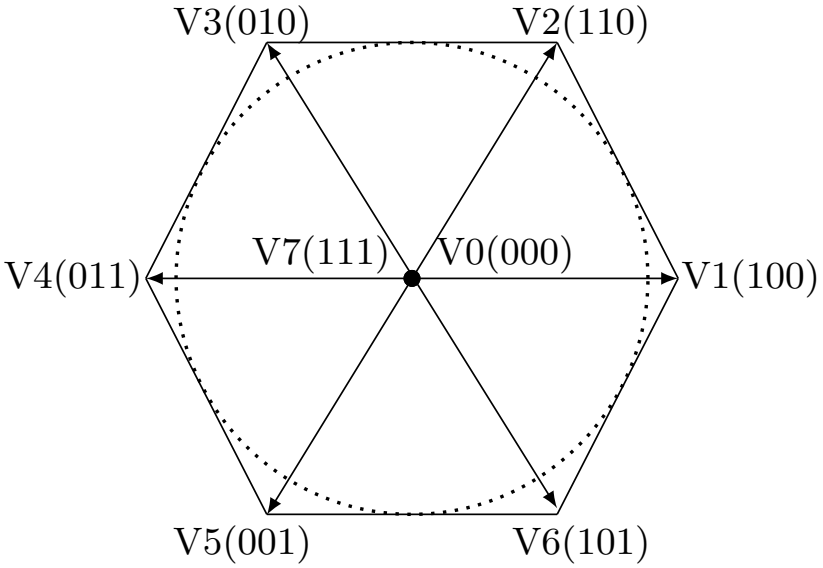

Figure 1.6: Voltage space vector structure of a three phase inverter.

synchronously rotating flux. In a variable frequency drive (VFD) the rotating flux within the machine is created by the voltage applied from a three phase inverter, consisting of six switches S_1 to S_6 as shown in Figure 1.5. Because of the complementary operation of switches (top and bottom switches are not turned ON together) of each inverter leg, altogether a three-phase, two-level inverter can have eight switching states. When all the top switches (S_1, S_3, S_5) or all the bottom switches (S_2, S_4, S_6) are ON, it results in zero output voltage as the load gets disconnected from the DC source. These are called null states of the inverter and the corresponding voltage vector is denoted as V_0(000) and V_7(111). The remaining six switching states are called active states, that results in six active voltage vectors V_1 to V_6 of magnitude V_{dc} with specific orientation as shown in Figure 1.6. The active voltage vectors V_1 to V_6 lie on the vertices of a hexagon while the null vectors or zero vectors (V_0 and V_7) lie at the center. The triplets like (100) shown in Figure 1.6 indicate the switching states in three legs of the inverter corresponding to a voltage space vector. '1' indicates the 'ON' status and '0' indicates 'OFF' status of the top switch in an inverter leg. For example in the triplet '100' the 1^{st} bit '1' indicates A-phase top switch is 'ON', 2^{nd} bit '0' indicates B-phase bottom switch is 'ON' while the 3^{rd} bit '0' indicate C-phase bottom switch is 'ON'. The basic idea of SVPWM technique is to establish a rotating voltage space vector closer to the idealized one

(continuously rotating) using the six active voltage vectors (V_1 to V_6) and two zero voltage vectors (V_0 and V_7). Any reference voltage vector of specific magnitude and orientation within the hexagonal structure is created in an average sense by switching the nearest three voltage vectors of the inverter for specific durations (dwell times) following the principle of volt-second balance.

1.2.2 Direct AC to AC converter fed drives

Cyclo-Converter fed drive

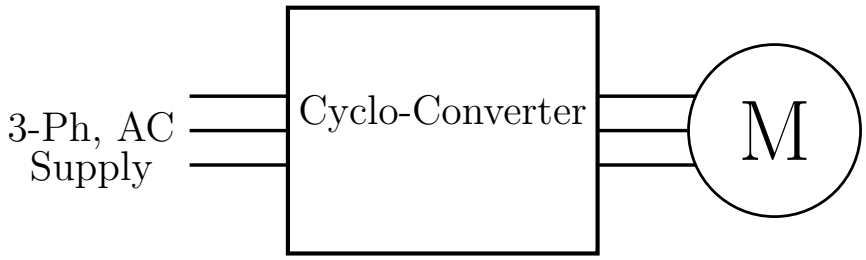

Figure 1.7: Block diagram of cyclo-converter based drive.

Cyclo-converters are popularly used in high-power (above 5MW), low speed applications for driving induction motor or synchronous motor [24, 25, 26, 27, 28]. It is a direct AC-AC converter fed drive marked by the absence of intermediate energy storage, as shown in Figure 1.7. The efficiency of this drive system is high due to the absence of intermediate energy storage element in the power converter. The major disadvantages of cyclo-converter fed drives are poor input power factor, complex converter structure, and the limit on the output frequency (limited to 45% of the line frequency) [29].

1.2.3 Current Source Inverter fed drives

The basic structure of a current source inverter (CSI) fed AC motor drive is shown in Figure 1.8. The input side converter is usually a controlled rectifier which along with a large inductor in series constitutes a current source. Controlled rectifiers are usually built using silicon controlled rectifiers (SCR) especially in high power applications. Closed loop operation of the controlled rectifier is a requirement in order to maintain the inductor current at a constant value. The current source inverter is built using voltage bi-directional

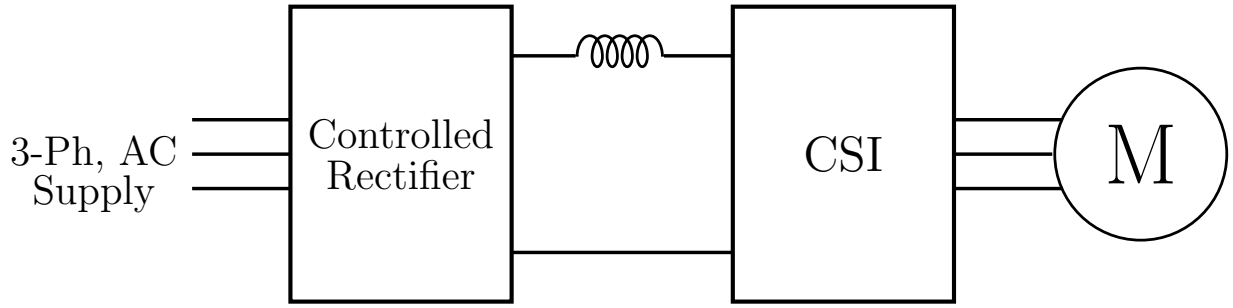

Figure 1.8: Block diagram of CSI fed AC motor drives.

two quadrant switches which block voltages of both polarities in the OFF state but conduct current only in one direction in the ON state. Though fully controlled devices like the gate turn off thyristor (GTO) and integrated gate commutated thyristor (IGCT) are used for building current source inverter in some applications, the high power drives segment is still dominated by SCRs.

The current source inverter fed drive is well suited for high power applications because of the advantages like inherent short circuit protection, easy four quadrant operation and low $\frac{dv}{dt}$ stress [30, 31, 32]. However, compared to the VSI fed drives the dynamic response of the CSI fed drive will be slower due to the large series inductor employed for building the current source. The CSI in these drives is operated in quasi square wave mode in high power applications. Selective harmonic elimination (SHE) and other pulse width modulation (PWM) schemes are also used for the control of the CSI [33, 34, 35, 36, 37, 38]. As already stated SCRs are commonly used in current source inverter fed drives used in high power applications. However the SCR is a semi-controlled device which can only be turned ON using the gate. External circuit is required to turn OFF or commutate a SCR which increases the complexity of the system. In certain applications where the load power factor can be leading, it is possible to use load itself for commutation of the SCRs. This process of turning OFF a SCR is known as load commutation. The synchronous motor can be operated at leading power factor by resorting to over-excitation. Hence, the load commutated SCR based CSI fed synchronous motor drive became very popular in the industry especially in high power drive applications. More details of the load commutated SCR based CSI fed drives are presented in the subsequent sections.

1.3 Load Commutated Inverter (LCI) fed drive

Even though the LCI fed drives come under the category of CSI fed drives, it is altogether treated as a different class of MV drives by the industry. It is one of the oldest topologies used in the area of high-power high-speed drive applications, which employs SCR as the semiconductor device for both machine side and line side converters. This topology is specifically used for synchronous motor drives. Even with significant improvement in the semiconductor technology SCR of thyristor family remains to be the only device available at very high power levels. Thus this topology remains to be the most preferred configuration when the power levels goes to tens of mega-watts [39, 40, 41, 42]. The block diagram of the load commutated inverter fed synchronous motor drive is shown in Figure 1.9. The line commutated SCR based rectifier in series with a large inductor is used to realize the current source. The machine side converter is a load commutated SCR based CSI operated in 120 degree conduction mode thereby causing the motor current to be quasi-square wave in shape. In the CSI, the load commutation is achieved by operating the synchronous motor in over-excited state. The back-EMF of the motor facilitates natural commutation of the SCR thereby obviating the need for a forced commutation circuit. The drive system hence is extremely simple and rugged [43]. As SCR is a highly rugged device in terms of its transient current ($\frac{di}{dt}$) and voltage ($\frac{dv}{dt}$) handling capabilities, the reliability of the system is very high. Other advantages of the drive include, reduced switching losses owing to 120 degrees mode of CSI operation and lesser conduction losses due to the low ON state voltage drop of the SCRs which is typically around 1.5V to 2V (even at higher currents of the order of 1000A it seldom exceeds 3V). This makes the efficiency of the drive very high close to 99% thereby bringing down the running cost. Another, main advantage is the reduced cost of the drive as the SCR remains to be a cheaper semiconductor device compared to the cost of the other semiconductor switching devices. Presently these drives are available in the market up to 100MW (in special cases even up to 150MW) [44, 45] and are very popularly used as high power drives in mining industries, oil and gas industries etc.

Some of the limitations of this drive are:

- Slow dynamic response due to the large inductor used in realizing the current

source. So its application is limited to areas like fans, pumps, etc. which do not demand high dynamic response.

- The starting of the drive is still a major challenge as the motor back-EMF would be insufficient for turn OFF process (commutation) of the SCR. Alternatively, a method called 'pulsed mode operation' or 'DC-link current pulsing' is used for starting of the drive as well as for its low speed operation[46, 47, 48]. But, this method results in large torque pulsations in the motor.

- Because of the 120 degree mode of CSI operation, the motor current is quasi square wave in shape, rich in lower order harmonics especially the 5^{th} and 7^{th} harmonics. This will result in large 6^{th} harmonic torque pulsations. This becomes significant at lower frequencies and if the frequency of the torque pulsations matches with the mechanical natural resonance frequency, it can cause extensive damage to shaft, coupling, etc. of the drive.

- Another limitation is that the topology is specific for synchronous motors and it cannot be used for induction motors which normally operate at lagging power factor.

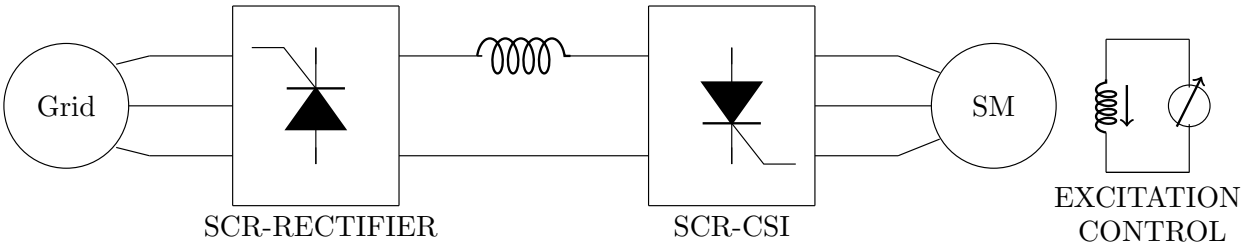

Figure 1.9: Block diagram of load commutated inverter fed synchronous motor drive.

1.4 Advantages of Induction Motors

Induction motors are extensively used in industrial applications. Over 70% of the industrial drives are induction motors, and they are considered to be far superior to the synchronous motor because of the following advantages.

- A squirrel cage induction motor has simple construction and it can be deployed in extremely harsh environments.
- It is almost a maintenance free motor.
- It is cheaper compared to the other motors.
- It has low weight and inertia for a given power.

1.5 Current Source Inverter fed Induction Motor Drive for High Power Applications

The current source inverter fed drives are preferred in many high power applications due to their advantages like inherent short circuit protection and capability to do regenerative braking without any additional hardware. The CSI fed induction motor drives were realized either based on forced commuted SCRs or self commutated devices such as GTO. Auto sequential commutated inverter (ASCI) was one such forced commutation based circuit [49, 50], that was used for induction motor drives, which employed SCRs as the switching devices. However a major problem encountered in the ASCI was the premature failure of capacitors due to which the industry stopped using ASCI fed drives. Later GTO based converter topologies were used for CSI fed induction motor drives [51]. It covered the low end of high power range since the maximum power rating of GTO was limited. Block diagram of GTO based CSI fed induction motor drive is shown in Figure (1.10). At the motor terminal a small snubber capacitor is required to absorb the commutation voltage spikes, but it is not shown in the block diagram. The GTO based drive is either operated in six-step mode or in PWM mode (by introducing notches at desired instants). The drive with six-step operation was widely used in multi-MW drives especially in the areas of pump and fan type applications. The major drawback of using GTO is its complex gate driver design. The negative gate current required for turn OFF of GTO was very high compared to the positive gate current required for its turn ON. Usually, the negative gate current would be in the order of $\frac{1}{5}$ to $\frac{1}{3}$ times of the anode current, ie. for a GTO with ON state current of 1000 A the magnitude of negative gate current required for turn OFF

is in the order of several hundred amperes [52, 53, 54]. This makes the design of gate driver circuit very complex because it may be necessary to have several high gain transistors in the driver circuit. Later, GTO was replaced by IGBTs with series diodes mostly at the low end of high power range. Since there was a lack of proper topology for CSI fed induction motor drives for high power applications the researchers in this field started exploring the possibility of developing load commutated SCR based CSI fed IM drive. As a result new topologies of SCR based CSI fed induction motor drives were proposed as presented in the following section.

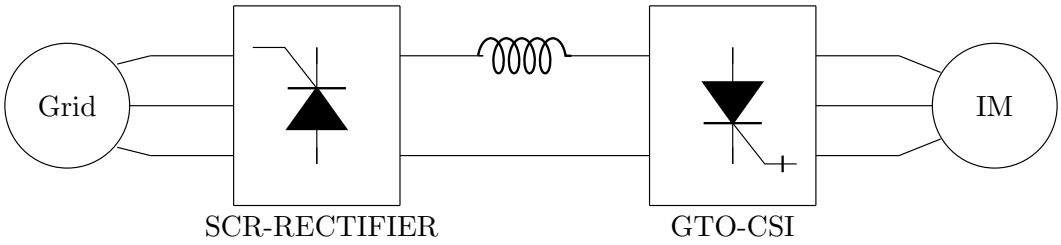

Figure 1.10: Block diagram of GTO based CSI fed induction motor drive.

1.6 Load commutated SCR based CSI fed induction motor drives

The concept of load commutation was applicable only for leading power factor loads. As such induction motors cannot be used in the conventional load commutated SCR based CSI schemes since it can operate only at lagging power factor. Initially the schemes with capacitor banks connected at the terminals of induction motor were used to realize load commutated SCR based CSI fed IM drives [55]. Figure 1.11 shows the block diagram of such a scheme. But as the power rating of the induction motor increases, the reactive power requirement also increases which in turn necessitates large AC capacitors. Also, in the case of variable frequency drives there can be resonance between the capacitors and the machine inductances (both leakage inductance and magnetizing inductance), which will lead to failure of the drive. In addition starting and low speed operation of the drive will be difficult. Hence, researchers have proposed hybrid drive topologies consisting of both CSI and VSI to realize load commuted SCR based IM drive [56, 57, 58, 59, 60, 61,

62].

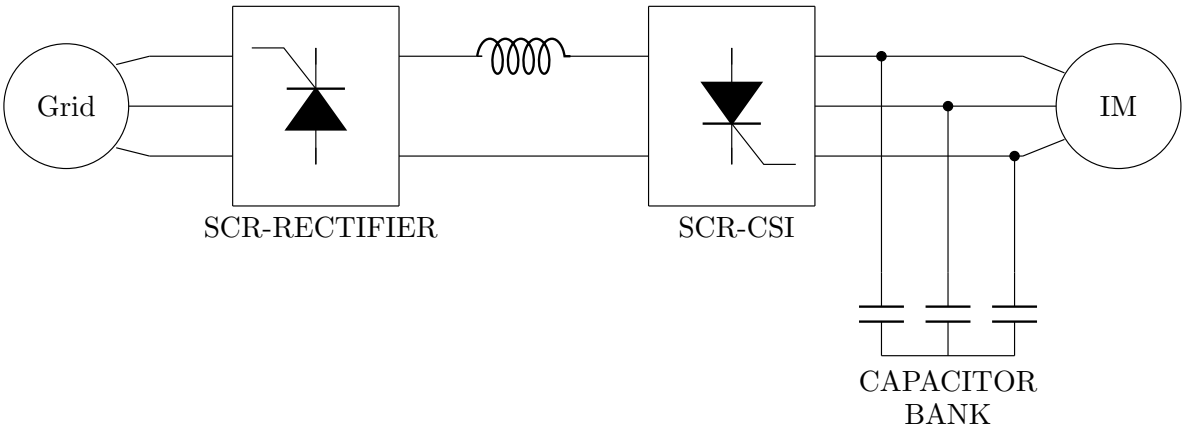

Figure 1.11: Block diagram of load commutated IM drive with capacitor bank.

1.7 Hybrid topologies using CSI and VSI for realization of load commutated SCR based IM drives

A few hybrid topologies consisting of both SCR based CSI and IGBT based VSI for realizing load commutated induction motor drive were reported in the literature. The basic idea in all such topologies is to make the power factor at the CSI terminals leading using a VSI connected at the motor terminals. The VSI in such schemes basically overcompensates the reactive power requirement of the induction motor thereby making the power factor leading at the CSI terminal. This idea of using VSI for reactive power compensation is originally derived from the concept of STATCOM used for reactive power compensation. As the CSI in the hybrid drive scheme is operated in 120 degree mode the motor current is quasi square wave in nature, rich in lower order harmonics. Therefore in most of the hybrid topologies VSI is also used for harmonic filtering to make the motor currents sinusoidal. A few hybrid topologies of load commutated SCR based IM drives are presented in [58, 59, 60, 56, 57]. The scheme presented in [58] has a shunt operated VSI connected at the motor terminal using an LC filter. The block diagram of this scheme is shown in Figure 1.12. In this configuration the VSI is operated in voltage controlled mode to provide reactive power and also as a harmonic filter for achieving sinusoidal motor currents.

Some of the drawbacks of the above scheme are listed below:

- The VSI requires a separate DC source, which needs an additional rectifier with capacitive filter and a transformer. This substantially increases the hardware complexity and the cost of the system.
- A separate interfacing arrangement (LC filter) is required for the VSI making the system bulky and expensive.
- The VSI operated in voltage control mode has limited capability to do harmonic filtering. So a large LC filter is also required to make the motor currents sinusoidal.

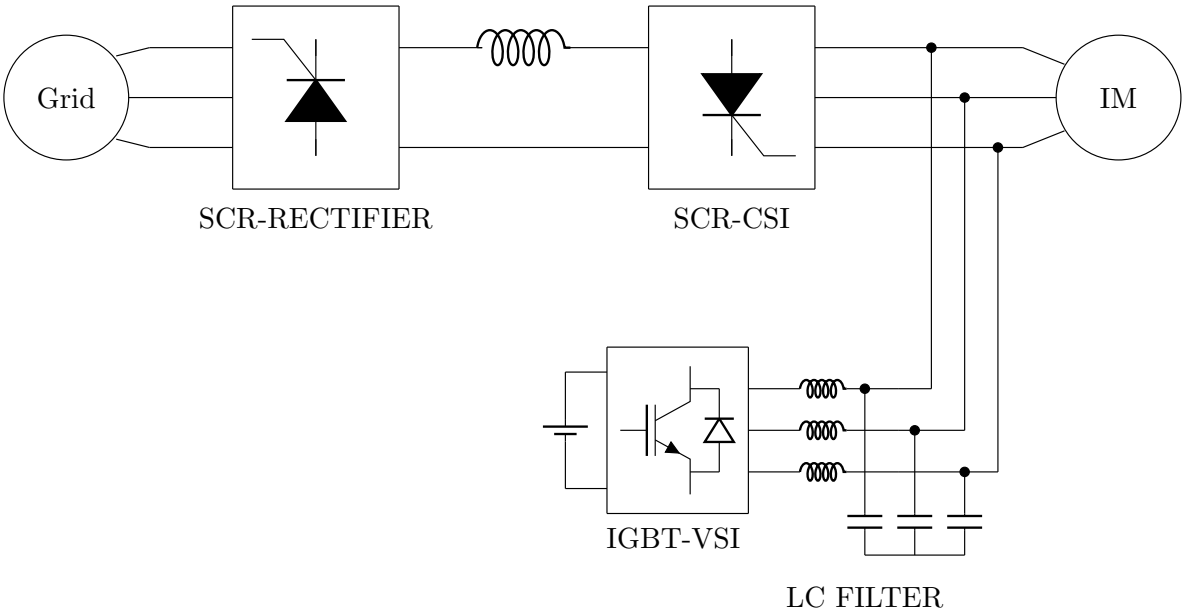

Figure 1.12: Block diagram of the hybrid scheme of load commutated SCR based induction motor drive with shunt connected IGBT based VSI.

In [59] the need of separate DC source for the VSI is avoided to make the system simpler. This hybrid configuration is similar to that shown in Figure 1.12, but instead of the line side SCR-based rectifier a diode bridge is used to provide constant voltage for the VSI and to a IGBT based buck converter. The buck converter generates the required variable voltage to realize the current source. Thus the buck converter enables both the VSI and CSI to be fed from a single diode bridge eliminating the need of separate DC source (with rectifier and transformer arrangement) for the VSI. But since the front-end

SCR based rectifier is replaced by a diode bridge the regeneration capability of the drive is lost which can be a serious drawback especially in high power applications. A configuration similar to that of Figure 1.12 is presented in [56]. In this scheme, with the help of current mode control of the VSI, a very high bandwidth active filter is created for current harmonic filtering thereby the bulky LC filter as required in [58] is avoided and instead only an interfacing inductor is used to connect VSI at the motor terminals. But still this configuration requires separate DC source for the VSI and an interfacing inductor thereby increasing the size, weight and cost of the system. In addition, to achieve sinusoidal motor currents in the complete range of speed, it is necessary to operate the VSI as a filter at a higher switching frequency which is not preferred in high power applications. The block diagram of a hybrid configuration for load commutated Active-Reactive Induction Machine (ARIM) presented in [57] is shown in Figure 1.13. ARIM is a specially designed induction motor which consists of two sets of three phase windings, a power winding and an excitation winding. The ARIM is specially designed for operation with load commutated SCR based current source inverter. In this scheme the SCR based CSI is connected to the high voltage power winding while the VSI is connected to the low voltage excitation winding using an LC filter arrangement. The basic idea of using ARIM is that the CSI would be used to provide the real power requirement of the motor while the VSI ensures load commutation of the CSI by providing adequate reactive power to the motor so as to make the power factor leading. The VSI operation also ensures reduction in torque pulsations due to current harmonics. The major drawbacks of this scheme are listed below:

- This scheme requires a specially designed induction machine (ARIM) and cannot be used for normal squirrel cage induction motor. Hence, retrofitting on the existing installations is not possible.

- The VSI requires separate DC source.

- The VSI is connected to the excitation winding (low-voltage winding) using an LC filter arrangement making the system bulky and expensive.

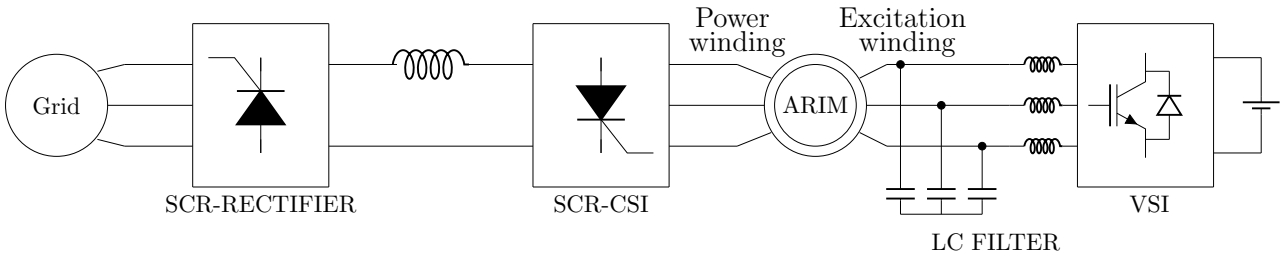

Figure 1.13: Block diagram of a hybrid CSI-VSI based configuration for load commutated Active Reactive Induction Machine.

1.8 Starting of the motor in hybrid IM drive topologies

In SCR based LCI fed synchronous motor drives, the motor back-EMF would be absent at the startup and insufficient during low speeds to perform load commutation of the CSI. Hence, a special mode of operation called 'pulsed mode' is required to run the motor till it reaches a minimum speed called 'change-over speed'. Generally, this change-over speed would be around 10-15% of the rated speed of the motor, so that the motor back-EMF would become sufficient for commutation of the SCRs. Similarly, a special mode of operation is adopted during starting in the hybrid CSI-VSI based LCI fed drive topologies discussed above. In these hybrid schemes the motor would be started and run using the VSI until motor reaches the change-over speed, as back-EMF would be insufficient for commutation. Only from the change-over speed onwards the CSI would be brought into operation.

The major drawbacks of such a starting scheme are:

- Since the motor is started and operated in the low speed regions using the VSI alone, a separate DC source for powering the VSI is required thereby making the system complex and expensive.
- Different control schemes are needed for the low speed and high speed operations of the drive. The VSI alone is used in the low speed region while in the high speed region both VSI and CSI are operational which makes the implementation of the control scheme complex.
- In the ARIM drive topology since the VSI is connected to the low-voltage excitation

winding, the drive cannot deliver rated torque at starting.

1.9 Major research contributions of the thesis

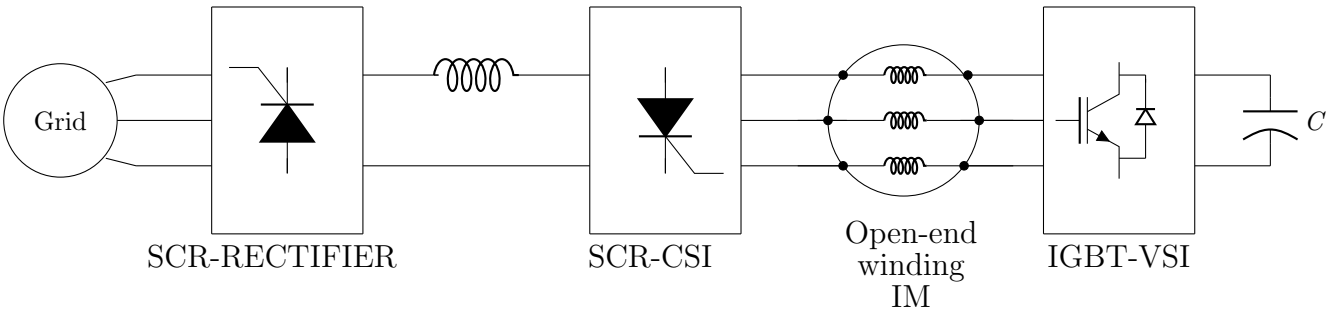

Figure 1.14: Block diagram of the proposed scheme of load commutated SCR based CSI fed IM drive with open end stator windings.

This research work addressed the problems in the field of CSI fed induction motor drives cited above and proposed new schemes for realization of load commutated SCR based CSI fed induction motor drives with open-end stator windings. The proposed schemes can be implemented on any induction motor by accessing both ends of the stator windings which are normally accessible through the terminal box fitted on the frame in all medium and high power induction motors. The concept of realization of multilevel voltage profile in an induction motor with open-end stator windings using two inverters connected at both ends of the stator windings was first introduced by Stemmler and Guggenbach in the year 1993 [63]. Since then a number of new topologies of voltage source multilevel inverters for induction motors with open-end stator windings have been proposed as reported in the literature [64, 65, 66, 67, 68, 69, 70, 71].

This research work for the first time explored the open-end stator winding configuration for realization of load commutated current source inverter fed motor drives. A new scheme for realization of load commutated SCR based current source inverter fed induction motor drive with open-end stator winding is proposed in this thesis. In this topology a SCR based CSI is connected at one end of the stator windings for feeding active power to the motor and a capacitor fed IGBT based VSI is connected at the end of the stator windings for supplying reactive power as depicted in Figure 1.14. Load commutation of the SCRs of the CSI is achieved by controlling the VSI in such a way that it over-

compensates the reactive power required by the motor so that at the CSI terminals the current leads ahead of the voltage. This scheme does not require any interfacing inductor or separate DC source for the VSI and can be implemented for any induction motor by accessing both ends of the stator windings. This topology is also free from problems like commutation failure at low speeds normally encountered in CSI fed high power drives. Since the CSI is used for supplying active power to the motor always this drive is capable of delivering the rated torque even at start-up. This drive system also facilitates easy regenerative braking without any additional hardware. Since, the VSI would be used for reactive power compensation alone its power rating would be far less compared to the CSI.

- In the proposed system the VSI requires only a capacitor to hold its DC link voltage. In contrast the VSIs of the systems presented in [58],[56],[57] require a separate DC source which substantially increases the hardware complexity, making the system bulky and expensive.
- The control scheme used in the proposed scheme is fundamentally different from that of [58],[59],[56],[57]. A current phasor oriented synchronously revolving reference frame based control scheme is developed for the proposed system taking motor current phasor as the reference.
- As mentioned earlier the current source inverter (CSI) cannot be used at start-up and during low speed operation of the induction motor in the existing hybrid topologies. Instead, the VSI is used for starting and running of the induction motor at low speeds. The CSI operation starts only when the motor speed exceeds certain value sufficient enough to generate adequate back EMF to commutate the SCRs in the CSI. Contrary to this, in the proposed system the CSI can be used for starting as well as running of the induction motor at all speeds.
- The proposed scheme can be implemented in the existing induction motor drives since both ends of the windings are generally accessible in almost all high power induction motors used in the industry.

Even in the proposed configuration, the torque pulsation due to lower order harmonics is

present because of the quasi square wave motor current. To improve the motor current profile, a load commutated multilevel CSI configuration is proposed for open-end winding IM in the second phase of the research work. This scheme consists of two isolated current source inveters operated in parallel with a phase shift. The basic idea of this configuration is to create a multilevel current profile in the machine winding instead of a quasi square wave current. With 30 degree phase shifted operation of CSIs a multi-stepped current is created to reduce the lower order harmonics especially the 5^{th} and 7^{th}. Even in the multilevel CSI scheme load commutation of both currents source inverters is achieved using VSI connected to the other end of stator winding of the open-end winding IM. With the reduction of 5^{th} and 7^{th} harmonics the 6^{th} harmonic torque pulsations would get reduced significantly.

In the third phase of the research work the concept of using VSI as a series compensator of reactive power is further extended to the traditional load commutated synchronous motor drive to address the issue of commutation failure during low speed operation due to insufficient back-EMF. In the traditional load commutated CSI fed synchronous motor drive 'pulsed mode' of operation is adopted during low speed operation and for the starting of the drive. But, this method of starting results in high torque pulsations in the motor. In the proposed scheme of load commutated open-end winding synchronous motor drive, normal load commutation is possible during the starting as well as in the low speed operating regions.

1.10 Organization of the Thesis

This thesis is organized as follows.

Chapter-2 : A new scheme for realization of load commutated SCR based current source inverter fed induction motor drive with open-end stator winding is presented in Chapter-2 of the thesis along with the theoretical concepts of the proposed scheme, the current oriented synchronously revolving reference frame based control scheme and the experimental results.

Chapter-3 : A new scheme for realization of a SCR based load commutated multilevel CSI configuration for an open-end winding induction motor is proposed in Chapter-3 of the thesis along with the theoretical concepts, control schemes, analysis and experimental results.

Chapter-4 : A new scheme to facilitate hassle-free load commutation of CSI fed synchronous motor drives during starting as well as at low speed without resorting to pulsed mode operation is proposed in Chapter-4 of this thesis along with theoretical analysis, control scheme and experimental results.

Chapter-5: Details of the experimental set up used for verification of the proposed drive schemes are presented in the chapter-5 of the thesis.

Chapter-6 concludes the thesis with a brief discussion on the further scope for research.

Chapter 2

Load-Commutated SCR-Based Current Source Inverter Fed Induction Motor Drive With Open-End Stator Windings

2.1 Introduction

This chapter deals with the proposed configuration of the load commutated SCR based current source inverter (CSI) fed induction motor (IM) drive with open-end stator windings. The block diagram of the proposed scheme is shown in Fig.1.14 of Chapter-1. The topology presented has a SCR based CSI connected at one end of the stator windings for feeding active power to the motor and a capacitor fed IGBT based voltage source inverter (VSI) connected at the other end of the stator windings for supplying reactive power. Load commutation of the SCRs of the CSI is achieved by controlling the VSI in such a way that it over-compensates the reactive power required by the motor so that at the CSI terminals the current leads ahead of the voltage. This scheme does not require any interfacing inductor or separate DC source for the VSI and can be implemented for any induction motor by accessing both ends of the stator windings. This topology is also free from problems like commutation failure at low speeds normally encountered in CSI fed high power synchronous motor drives. The proposed drive system is also capable of operating in all the four quadrants with easy regeneration.

2.2 Power circuit diagram of the proposed drive system

The power circuit diagram of the proposed scheme is shown in Figure 2.1. It consists of a SCR-based CSI at one end of the stator winding and an IGBT-based capacitor-fed VSI at the other end of the stator windings. The current source is realized using an SCR-based controlled rectifier with an inductor at the output. A closed loop control scheme

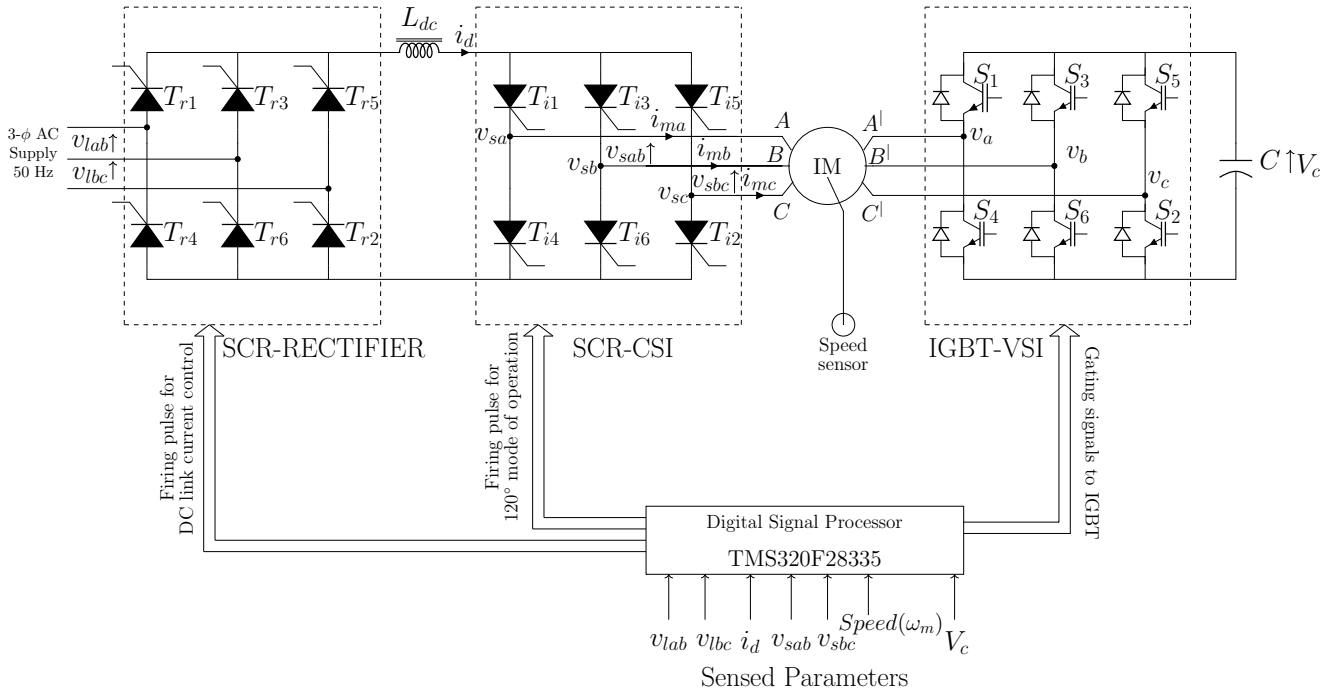

Figure 2.1: Power circuit diagram of the proposed scheme.

regulates the output of the current source by employing firing angle control of SCRs. The CSI is constructed using normal converter grade SCRs. The CSI switched at the fundamental frequency, is operated in 120 degrees conduction mode, resulting in a motor current having quasi-square wave shape.

The proposed load commutated drive system has the following subsystems. The names of the subsystems as marked in Figure 2.1, are given in brackets.

- Fully controlled line commutated SCR based AC to DC converter (SCR-RECTIFIER).
- Inductive filter (L_{dc}).
- Load commutated SCR based Current Source Inverter (SCR-CSI).
- Induction motor with open-end stator windings.
- Capacitor fed Voltage Source Inverter (IGBT-VSI).

These subsystems are described in the following sections.

2.2.1 Fully controlled line commutated SCR based AC to DC converter

The SCR based line commutated converter is used as phase controlled rectifier to generate the variable voltage required for realizing the current source. Figure2.2 shows the schematic diagram of the SCR based controlled rectifier. Since, SCRs in this converter are commutated by applying reverse voltage across them using the 3-phase AC supply lines, this rectifier is known as line commutated converter. The conduction periods of the SCRs (T_{r1} to T_{r6} in Figure2.2) are controlled to vary the output DC voltage 'V_{dc}', which in turn controls the DC-link current 'i_d' (Figure2.1). In order to perform proper triggering of SCRs of each leg, the triggering angle 'α' of the SCRs are generated in synchronization with that of the respective phase voltages. This is done by sensing the AC line voltages v_{lab}, v_{lbc}, using which the per-phase voltages v_{la}, v_{lb}, v_{lc} are derived by the following equations.

$$v_{la} = \frac{1}{3} \times (v_{lab} - v_{lca}) \tag{2.1}$$

$$v_{lb} = \frac{1}{3} \times (v_{lbc} - v_{lab}) \tag{2.2}$$

$$v_{lc} = \frac{1}{3} \times (v_{lca} - v_{lbc}) \tag{2.3}$$

Fig.2.3 shows the block diagram of the firing pulse generation scheme. The individual SCRs of each phase are triggered at a firing angle of 'α' degrees with respect to the positive zero crossing of the line voltage appearing across them (corresponds to the phase angle ωt=30° of the corresponding phase voltage). Fig.2.4 shows the firing pulse pattern (G_{Tr1} to G_{Tr6}) of SCRs along with their conduction period (T_{r1} to T_{r6}), drawn by taking A-phase supply voltage (v_{la}) as the reference. From this figure it can be observed that the A-phase top SCR T_{r1} is triggered by the gating pulse G_{Tr1} at ωt = (30+ α) degrees. It remains in conduction for 120 degrees after triggering. The bottom SCR of the same phase (T_{r4}) is triggered 180 degrees after triggering of the top SCR. Since the top and

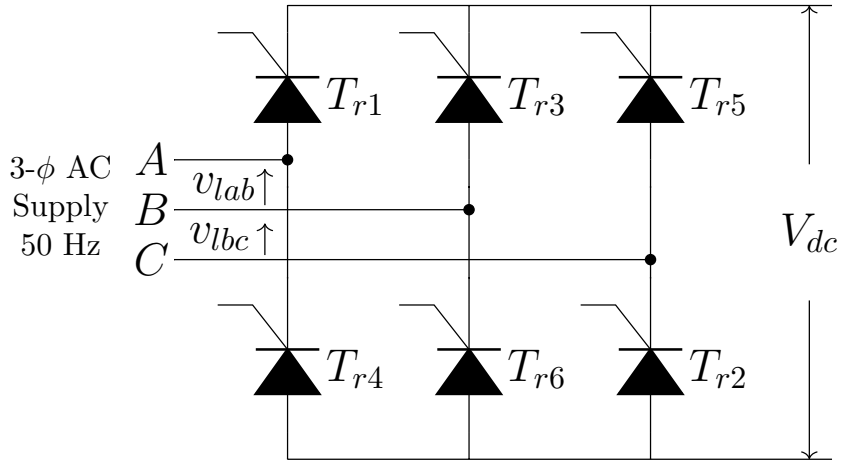

Figure 2.2: Line commutated SCR based rectifier.

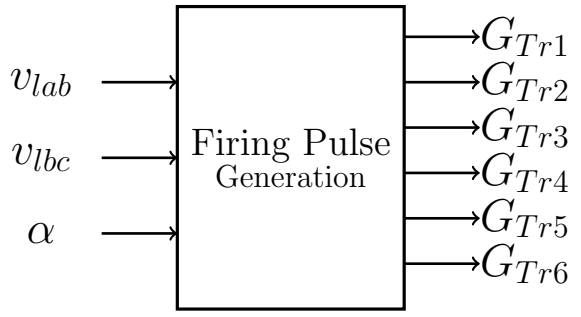

Figure 2.3: Firing pulse generation block diagram of line side converter.

bottom SCRs in a phase are triggered at an interval of 180 degrees they cannot conduct simultaneously. At any instant one top SCR of any phase and a bottom SCR of a different phase will be in conduction. It can be seen that the triggering sequence is: T_{r1}, T_{r2}, T_{r3}, T_{r4}, T_{r5}, T_{r6}. This operation results in six pulses in the output DC voltage over a period of the input voltage and hence this converter is also known as six pulse rectifier.
The expression for the DC output voltage in terms of the firing angle is given by:

$$V_{dc} = \frac{3\sqrt{2}V_L \cdot cos(\alpha)}{\pi} \tag{2.4}$$

where V_L is the RMS value of the input line voltage.
It can be seen from the above expression that if the triggering angle is less than 90 degrees the output DC voltage will be positive and if the triggering angle is greater than 90 degrees the output DC voltage will be negative. Since the output current (i_d) is always unidirectional this converter can be operated either in rectification or inversion mode.

When the firing angle is in the range:0 < α < 90 degrees,the converter operates in rectification mode, where both V_{dc} and i_d are positive and the power flows from AC side to DC side.
If the converter has a firing angle range:90 < α < 180 degrees, it operates in inversion mode, since the voltage V_{dc} is negative and i_d is positive and the power flow will be from DC side to AC side, provided DC side has a power source.
This feature of the line commutated SCR based converter is instrumental in regenerative braking of the drives in which the stored mechanical energy in the motor and the load is converted to electrical energy and fed back to the AC source.
Line commutated converter together with the DC-filter choke (L_{dc}) constitutes the current source.

2.2.2 Load commutated SCR based Current Source Inverter

Figure 2.5 shows the circuit diagram of load commutated SCR based current source inverter (CSI). It is connected to the stator terminals (A, B, C) at one side of the stator windings of the open-winding induction motor (IM) as shown in Figure 2.1. It consists

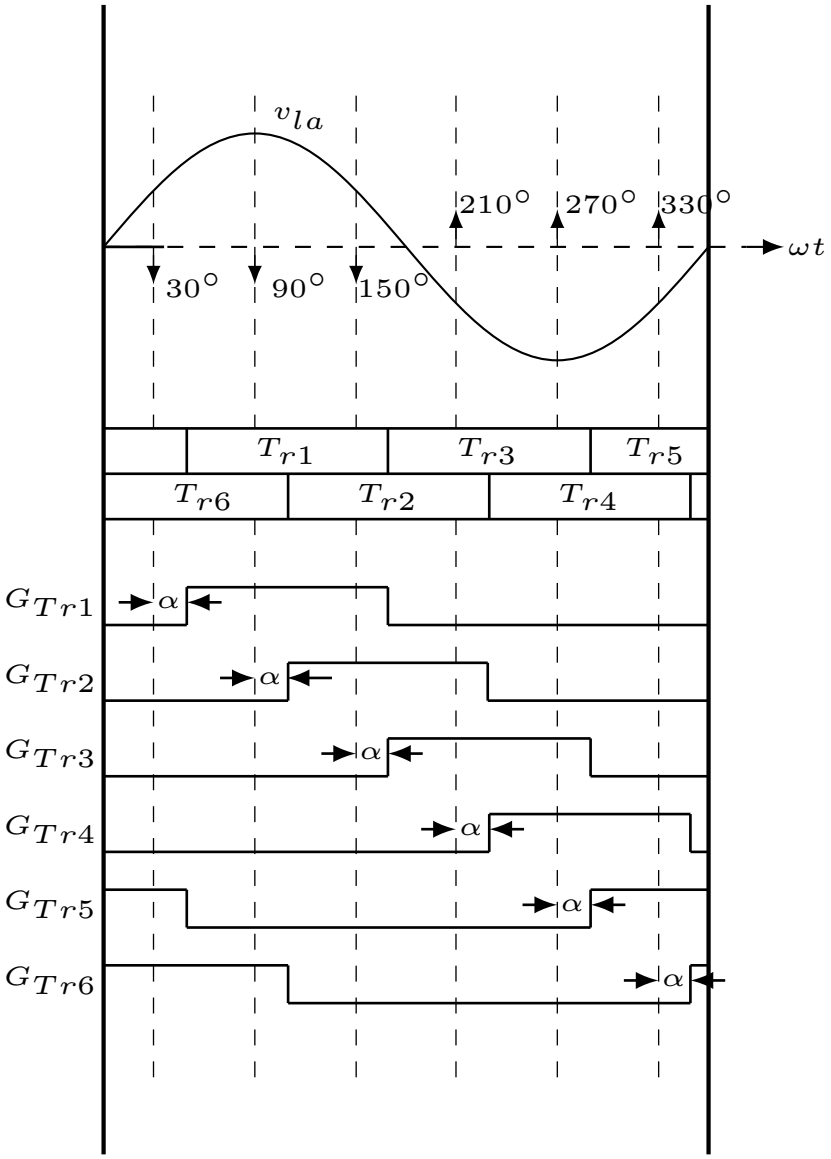

Figure 2.4: Rectifier SCR gating pulse pattern.

of six SCRs (T_{i1} to T_{i6}) which are triggered by the gating signals G_{Ti1} to G_{Ti6} respectively. The CSI is operated in 120 degree conduction mode, where each SCR conducts for a duration of 120 degrees, resulting in a motor current having quasi square wave shape as shown in Figure 2.6. In 120 degrees conduction mode of operation of the CSI, at any instant top SCR of one-phase and bottom SCR of another phase would be in conduction. However during the process of commutation one more SCR will be in conduction for the duration of the commutation interval as explained later. The conduction periods of the SCRs T_{i1} to T_{i6} and the corresponding gating signals G_{Ti1} to G_{Ti6}, drawn with respect to the fundamental component of A-phase motor current 'i_{maf}', are shown in Figure 2.7.

It can be observed from the figure that the top SCR of A-phase is triggered at ωt=30 degree and it conducts for a duration of 120 degrees, till ωt=150 degrees. Similarly, the bottom SCR of A-phase is triggered at ωt=210 degrees and it conducts till ωt=330 degrees. The top and bottom SCRs of the same phase are triggered with a phase shift of 180 degrees thereby establishing a quasi square wave motor current as shown in Figure 2.6.

The primary condition to be satisfied for the load commutation of the CSI is to operate it at a leading power factor. It means that the CSI phase current (or motor current) should lead ahead of the corresponding terminal voltage of the CSI. The CSI terminal voltages (v_{sa}, v_{sb}, v_{sc}) are the per-phase voltages defined with respect to the fictitious neutral point, as no physical neutral point exists in the system. The phase voltages of the CSI can be derived from its line voltages (v_{sab}, v_{sbc}, v_{sca}), which can be sensed, using the following equations, using the following equations.

$$v_{sa} = \frac{1}{3} \times (v_{sab} - v_{sca}) \tag{2.5}$$

$$v_{sb} = \frac{1}{3} \times (v_{sbc} - v_{sab}) \tag{2.6}$$

$$v_{sc} = \frac{1}{3} \times (v_{sca} - v_{sbc}) \tag{2.7}$$

The CSI terminal voltages (phase voltages: v_{sa}, v_{sb}, v_{sc}) derived from the sensed line

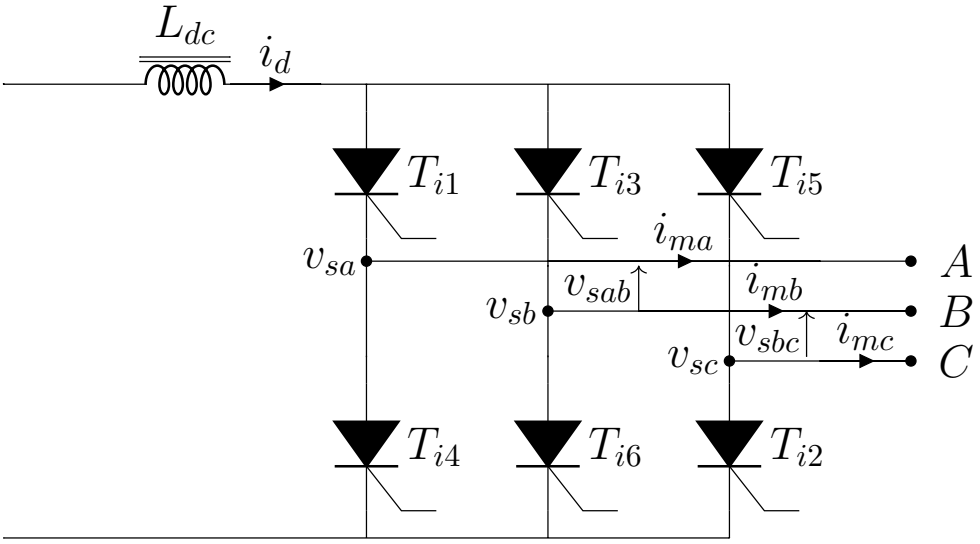

Figure 2.5: Circuit diagram of load commutated SCR based CSI.

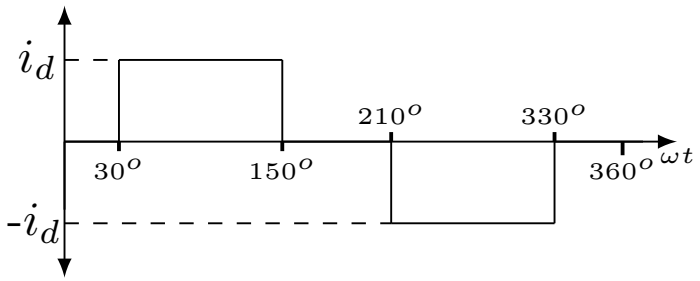

Figure 2.6: Per-phase CSI current or motor current.

voltages are used in the implementation of the control scheme as explained later in this chapter.

2.2.3 Capacitor fed Voltage Source Inverter

The voltage source inverter (VSI) connected to the stator terminals ($A^|$, $B^|$, $C^|$) of the open-end winding IM consists of six IGBTs (S_1 to S_6) . Since the VSI is used for reactive power compensation alone it does not require a DC power source as its voltage source, instead a voltage holding capacitor 'C' is employed for this purpose. The sinusoidal pulse width modulation (SPWM) technique is used for controlling this inverter.

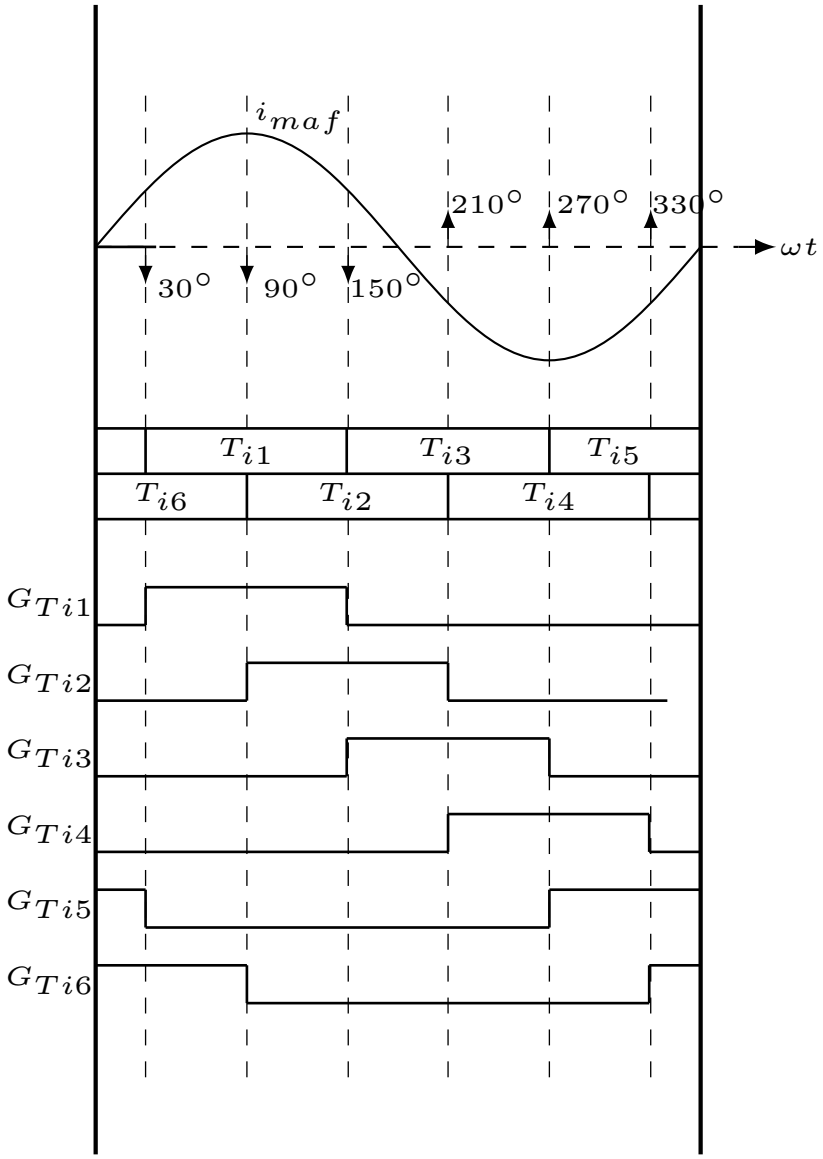

Figure 2.7: CSI SCR gating pulse pattern.

2.3 Load commutation in the proposed drive: Basic principles

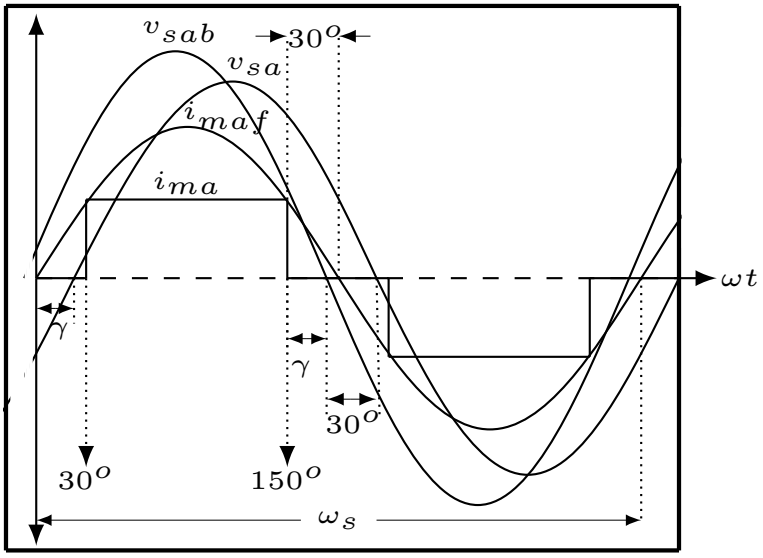

Figure 2.8: CSI terminal voltage (v_{sa}), CSI line voltage (v_{sab}), motor current i_{ma} and its fundamental component (i_{maf}) waveforms.

The new scheme proposed in this thesis enables load commutation of the current source inverter (CSI) fed induction motor drives even though the induction motor always operate at lagging power factor. The basic principle of the scheme is to operate the combined system of the induction motor and the VSI (Figure 2.1) at leading power factor, such that the CSI terminal voltage lags behind the fundamental component of the motor current by the required commutation angle. The concept is illustrated in the system phasor diagram shown in Figure 2.10. The role of VSI is to inject only reactive power into the system and maintain the lead angle γ radians. In this phasor diagram the motor voltage V_m leads ahead of the fundamental component of motor current (i_{mf}) by the machine power factor angle ϕ. The CSI terminal voltage phasor (V_s) is the phasor sum of the motor voltage (V_m) and the VSI voltage (V_v) as given in Equation 2.8.

$$\vec{V_s} = \vec{V_m} + \vec{V_v} \tag{2.8}$$

Thus the CSI terminal voltage phasor (V_s) is made to lag behind the fundamental component of motor current (I_{mf}) by an angle 'γ' as depicted in the phasor diagram

shown in Figure2.10. The VSI voltage (V_v) should be in quadrature with the fundamental component of motor current (I_{mf}) to ensure that the VSI exchanges only reactive power with the system. Since the VSI is not supplying any active power it does not require a separate DC power source. Instead a charged capacitor is sufficient to provide DC link voltage to the VSI. But in practical system there will be switching and conduction losses in the inverter and dielectric loss in the capacitor. These losses would cause dip in the capacitor voltage. Hence, a small amount of active power has to be drawn from the CSI in order to compensate for these losses so as to maintain the VSI capacitor voltage at the required level. This necessitates a closed loop control scheme to maintain the capacitor voltage at its reference value.

The process of load commutation can be explained with the help of Figure 2.8 which depicts the waveforms of the fundamental component of A-phase CSI terminal voltage (v_{sa}), fundamental component of CSI line voltage v_{sab}, motor current (i_{ma}) and fundamental component of motor current (i_{maf}). The A-phase top SCR (T_{i1}) is triggered at ωt= 30 degrees which would be in conduction for a period of 120 degrees till ωt= 150 degrees. When the top SCR of any phase is conducting the bottom SCR of another phase also will be in conduction. It can be seen from Figure 2.7 that when the A-phase top SCR (T_{i1}) is conducting from ωt= 30 degrees to ωt= 150 degrees, the bottom SCR of B-phase (T_{i6}) is in conduction from ωt= 30 degrees to ωt= 90 degrees and the bottom SCR of C-phase (T_{i2}) is in conduction from ωt= 90 degrees to ωt= 150 degrees. When the CSI operates at leading power factor the fundamental component of motor current i_{maf} leads ahead of the fundamental component of the CSI terminal voltage (v_{sa}) by an angle γ radians, as shown in Figure 2.8. Also, the CSI line voltage v_{sab} leads ahead of the CSI terminal voltage v_{sa} by an angle of 30 degrees, as marked in Figure 2.8. At the instant ωt= 150 degrees B-phase top SCR (T_{i3}) is triggered, causing the reverse line voltage v_{sab} to appear across the top SCR T_{i1} of A-phase which is in conduction. Figure 2.9 shows the state of the CSI circuit during the commutation of the A-phase top SCR (T_{i1}).

Three SCRs; A-phase top SCR T_{i1}, B-phase top SCR T_{i3} and C-phase bottom SCR T_{i2} will be in conduction during the commutation interval. As already stated the CSI terminal voltage v_{sa} is made to lag behind the fundamental component of motor current i_{maf} by angle 'γ' radians. For proper commutation the line voltage v_{sab} should remain

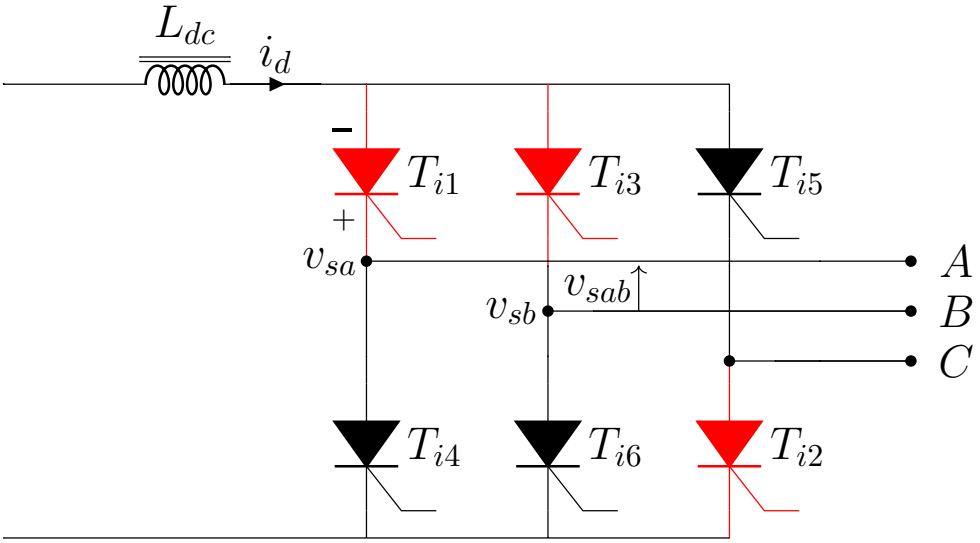

Figure 2.9: Circuit state at the commutation of A-phase top SCR T_{i1}.

positive for a duration '$\frac{\gamma}{\omega_s}$' to ensure that the reverse voltage (v_{sba}) appears across the outgoing SCR T_{i1}, where ω_s is the operating frequency of the drive in radians / seconds. The duration '$\frac{\gamma}{\omega_s}$' should be greater than the turn OFF time of the SCR. In other words, from the instant ωt = 150 degrees to ωt = (150+γ) degrees the line voltage v_{sab} appears as negative voltage across the SCR T_{i1} thereby facilitating the commutation. The polarity of reverse voltage that appears across T_{i1} is marked in Figure 2.9. Similar process is followed in commutation of all other SCRs. Table-2.1 shows the list of CSI line voltages (v_{sab}, v_{sbc}, v_{sca}), that facilitate the commutation of all the six SCRs of the CSI (T_{i1} to T_{i6}).

Table 2.1
List of line voltages that facilitates commutation of SCRs (T_{i1} to T_{i6}) of CSI

Time(in degree)	Outgoing SCR	Incoming(or triggered) SCR	Line voltage that facilitates turn OFF
ωt=30 degree	T_{i5}	T_{i1}	v_{sca}
ωt=90 degree	T_{i6}	T_{i2}	v_{scb}
ωt=150 degree	T_{i1}	T_{i3}	v_{sab}
ωt=210 degree	T_{i2}	T_{i4}	v_{sac}
ωt=270 degree	T_{i3}	T_{i5}	v_{sbc}
ωt=330 degree	T_{i4}	T_{i6}	v_{sba}

In Fig. 2.8 at ωt=150 degrees, the motor current waveform (i_{ma}) is shown as perfect quasi square wave where the change in the current levels are instantaneous, which is an ideal case. In practical converters rising and falling of the current will not be instantaneous

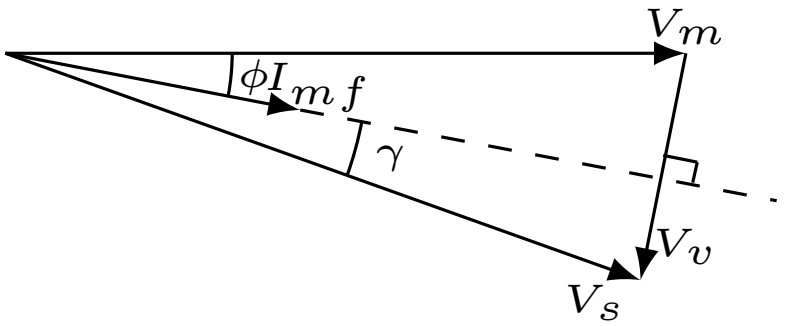

Figure 2.10: System phasor diagram representing the motor voltage (V_m), VSI voltage (V_v) and the CSI terminal voltage (V_s)

since turn ON and turn OFF process of the SCRs take finite time. Hence the rising of the current will be with a slope of duration equal to the turn ON time and the current falls to zero with a slope of duration equal to the turn OFF time of the SCR. As described earlier the lead angle 'γ' has to be more than the turn-OFF time of the SCR. The turn OFF time depends on the type of SCR used for building the CSI. There are two types of SCRs, classified based on the turn OFF time, namely:

1. Converter grade SCR

2. Inverter grade SCR(fast switching SCR)

The converter grade SCRs are slow operating devices having high turn OFF time (t_q) in the range of 50 to 100 μsec. They are widely used in line commutated converters where the turn OFF happens through natural commutation. The inverter grade SCRs have low turn OFF time compared to the converter grade type, typically in the range of 3 to 50 μsec. So the condition to be satisfied for load commutation is that the lead angle time '($\frac{\gamma}{\omega_s}$)' has to be greater than the turn OFF time 't_q'.

$$\frac{\gamma}{\omega_s} > t_q \tag{2.9}$$

Hence, 'γ' is to be chosen such that it satisfies the Eq.(2.9) during the complete range of motor operation.

2.4 Control Scheme of the proposed load commutated IM drive

The control scheme of the proposed load commutated IM drive system mainly involves the control of the current source inverter for achieving the required performance of the motor and the control of the voltage source inverter to facilitate load commutation. In addition, the rectifier at the input side needs to be controlled to provide the required current for the CSI and also to facilitate reverse power flow during regenerative braking. The control schemes are described in the following sections.

2.4.1 Current Source Inverter Control Scheme

The speed control of the motor is performed by varying the DC-link current (i_d) and the operating frequency of the CSI. The basic control scheme of the CSI is depicted in Figure 2.11. The speed controller compares the actual speed of the motor (ω_m) with the speed reference(ω_{ref}) to generate the slip speed ω_{slip}. The range of variation in the slip speed is limited by the slip limit block. The DC-link current reference is generated based on the slip speed to enable the motor to deliver the torque demanded by the load. The DC-link current to be maintained is obtained from the current reference block which is basically a look up table consisting of the RMS values of the fundamental component of the motor current(i_{mrms}) for different values of slip. The RMS value of the fundamental component of the motor current, as a function of the DC-link current i_d, can be obtained from the Fourier series expansion of the actual motor current(i_m):

$$i_m = \frac{2\sqrt{3}}{\pi} i_d [sin(\omega t) - \frac{1}{5} sin(5\omega t) + \frac{1}{7} sin(7\omega t) + ...] \tag{2.10}$$

The RMS value of the fundamental component of the motor current i_{mrms} can be expressed as :

$$i_{mrms} = \frac{\sqrt{6}}{\pi} \cdot i_d \tag{2.11}$$

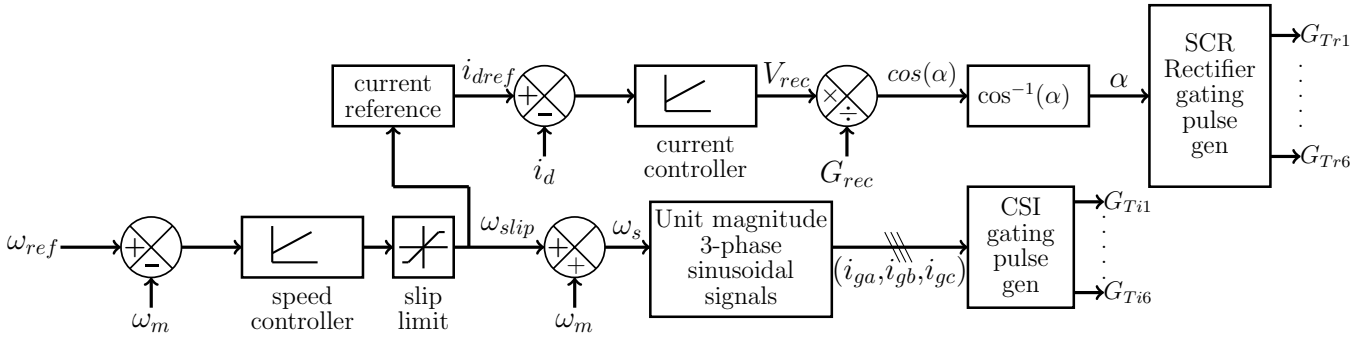

Figure 2.11: CSI control scheme

The DC-link current reference (i_{dref}) to be maintained can be obtained from Equation (2.11). This DC-link current reference is maintained by the current controller by controlling the firing angle α of the rectifier. The firing angle is obtained by dividing the current controller output (V_{rec}) with the rectifier converter gain (G_{rec}). The average output voltage of the rectifier as a function of firing angle α is as given below.

$$V_{dc} = \frac{3\sqrt{3}V_m \cdot cos(\alpha)}{\pi} \tag{2.12}$$

where, V_m is the peak value of the per-phase supply voltage.
The rectifier gain G_{rec} can then be written as,

$$G_{rec} = \frac{3\sqrt{3}V_m}{\pi} \tag{2.13}$$

The firing angle 'α', so obtained is used for generating the gating pulses (G_{Tr1} to G_{Tr6}) of the SCRs (T_{r1} to T_{r6}) of the rectifier.

The operating frequency of the CSI (synchronous frequency (ω_s)) for a given motor speed is obtained by adding the slip speed (ω_{slip}) and the actual motor speed (ω_m). Using the synchronous frequency (ω_s) information, 120 degree phase shifted, three phase sinusoidal signals(i_{ga}, i_{gb}, and i_{gc}) of unit magnitude shown in Figure 2.12 are generated by the 3-phase sinusoidal signal block generator.

$$i_{ga} = 1 \cdot sin(\omega t) \tag{2.14}$$

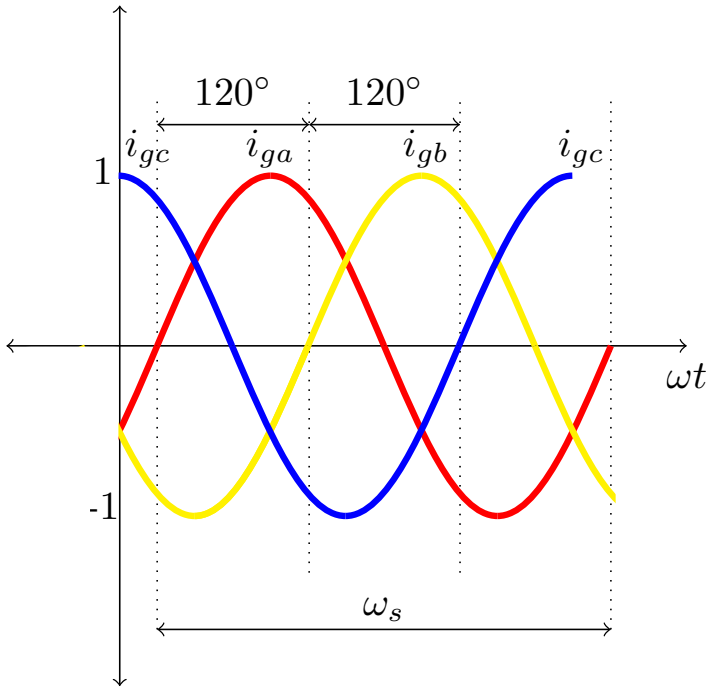

Figure 2.12: Unit magnitude three phase sinusoidal signals for CSI gate pulse generation

$$i_{gb} = 1 \cdot sin(\omega t - 120^{\circ}) \tag{2.15}$$

$$i_{gc} = 1 \cdot sin(\omega t - 240^{\circ}) \tag{2.16}$$

The gating pulses (G_{Ti1} to G_{Ti6}) of the SCRs of the CSI are generated using the three phase sinusoidal signals (i_{ga}, i_{gb}, and i_{gc}) of unit magnitude, for operating the CSI in 120 degrees conduction mode. The implementation of CSI control scheme is shown in Figure 2.13.

2.4.2 Voltage Source Inverter Control Scheme

The role of the VSI is to facilitate load commutation of the CSI, by keeping the fundamental component of the motor current leading ahead of the CSI terminal voltage under all conditions of motor operation. This necessitates the operation of the VSI and the CSI in synchronism. The control scheme for the VSI is implemented on a synchronously ro-

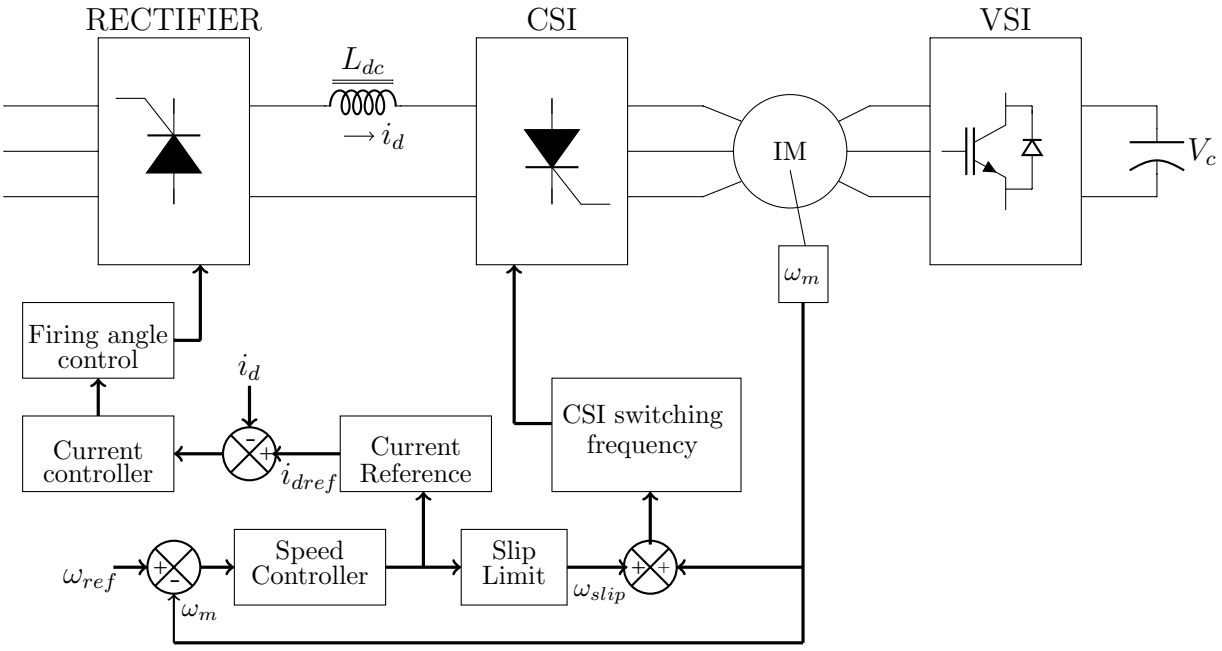

Figure 2.13: Implementation of CSI control scheme

tating (d-q) reference frame with d-axis oriented along the motor current phasor (I_{mf}). The fundamental components of three phase motor currents i_{maf}, i_{mbf} and i_{mcf} which are required for three phase (abc) to d-q transformation can be obtained from the unit magnitude three phase sinusoidal signals of the CSI (i_{ga},i_{gb},i_{gc}) and the DC-link current(i_d). From the Fourier series expansion of the motor current i_m given in Equation 2.10, the fundamental component of the motor current i_{mf} can be obtained as in Equation 2.17.

$$i_{mf} = \frac{2\sqrt{3}}{\pi} \cdot i_d \cdot sin(\omega t) \tag{2.17}$$

The fundamental components of the motor current in A-phase, B-phase and C-phase(i_{maf}, i_{mbf} and i_{mcf} respectively) would be in phase with the unit magnitude three phase sinusoidal signals i_{ga}, i_{gb}, i_{gc} respectively. So, the fundamental component of three phase motor currents can be written as:

Fundamental component of A-phase motor current:

$$i_{maf} = \frac{2\sqrt{3}}{\pi} \cdot i_d \cdot i_{ga} \tag{2.18}$$

Fundamental component of B-phase motor current:

$$i_{mbf} = \frac{2\sqrt{3}}{\pi} \cdot i_d \cdot i_{gb} \tag{2.19}$$

Fundamental component of C-phase motor current:

$$i_{mcf} = \frac{2\sqrt{3}}{\pi} \cdot i_d \cdot i_{gc} \tag{2.20}$$

The fundamental components of three phase motor currents i_{maf},i_{mbf} and i_{mcf} are used for abc to $\alpha - \beta$ (stationary frame) transformation, to obtain the α-axis, β-axis components '$i_{mf\alpha}$' and '$i_{mf\beta}$' of the motor current respectively, using Equation (2.21).

$$\begin{bmatrix} i_{mf\alpha} \\ i_{mf\beta} \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{maf} \\ i_{mbf} \\ i_{mcf} \end{bmatrix} \tag{2.21}$$

Using $i_{mf\alpha}$ and $i_{mf\beta}$ the unit vectors (sin(θ) and cos(θ)) required for transformation to d-q reference frame can be derived using Equation (2.22) and Equation (2.23).

$$sin(\theta) = \frac{i_{mf\beta}}{\sqrt{{i_{mf\alpha}}^2 + {i_{mf\beta}}^2}} \tag{2.22}$$

$$cos(\theta) = \frac{i_{mf\alpha}}{\sqrt{{i_{mf\alpha}}^2 + {i_{mf\beta}}^2}} \tag{2.23}$$

Also, the terminal voltages of the CSI (v_{sa}, v_{sb} and v_{sc}) derived from the sensed CSI line voltages (v_{sab}, v_{sbc} and v_{sca}) are transformed to d-q reference frame (rotating reference frame) to obtain the d-axis and q-axis components, 'V_{sd}', 'V_{sq}' respectively. The expressions for abc to α-β transformation and the α-β to d-q transformation of the voltages are given in Equation (2.24) and Equation (2.25) respectively. A low pass filter (LPF) is used for extracting the fundamental components V_{sdf} and V_{sqf} of V_{sd}, V_{sq} respectively.

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.24}$$

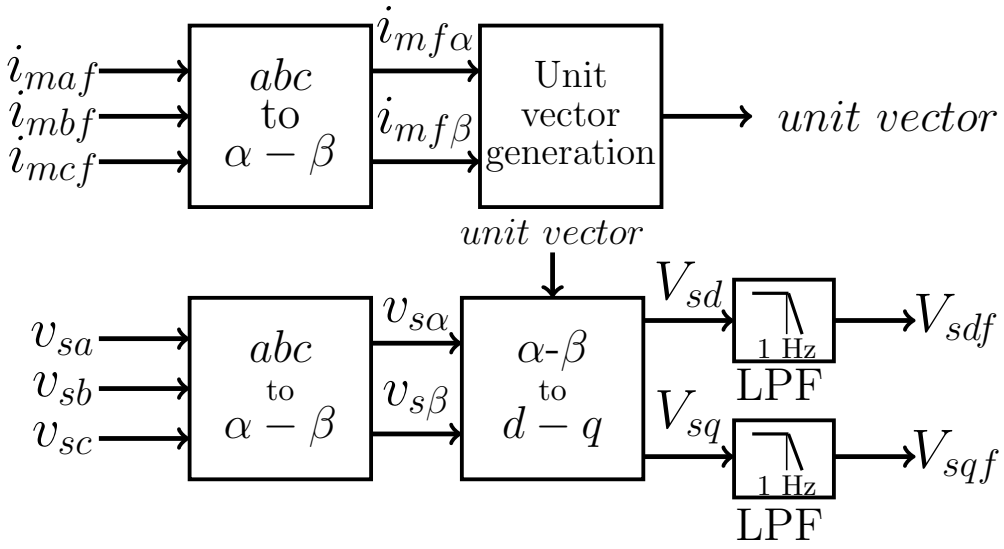

Figure 2.14: The block diagram showing the transformation of the fundamental component of motor currents (i_{maf},i_{mbf} and i_{mcf}) and the CSI terminal voltages (v_{sa}, v_{sb} and v_{sc}) from abc to d-q frame of reference

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{2.25}$$

Figure 2.15 shows the phasor diagram where the motor current phasor 'I_{mf}' leads the CSI terminal voltage phasor 'V_s' by angle 'γ'. The filtered values of the d-axis and q-axis components (V_{sd}, V_{sq}) are extracted using a low pass filter (LPF) having cut-off frequency of 1Hz. The transformations of the parameters from abc to d-q frame and the DC-component extraction are shown in Figure 2.14. The DC-components (V_{sdf}, V_{sqf}) of V_s are marked in Figure 2.15. The relationship between V_{sdf} and V_{sqf} as a function of lead angle 'γ' is given by Equation(2.26). The operation of the VSI should ensure that this ratio between V_{sdf} and V_{sqf} is maintained always to make the motor current lead ahead of the CSI terminal voltage by an angle 'γ'. The complete control scheme of VSI is shown in Figure 2.16. It basically consists of two controllers, q-axis controller for reactive power compensation and the d-axis controller to maintain the capacitor voltage at the required level.

$$tan(\gamma) = \frac{V_{sqf}}{V_{sdf}} \tag{2.26}$$

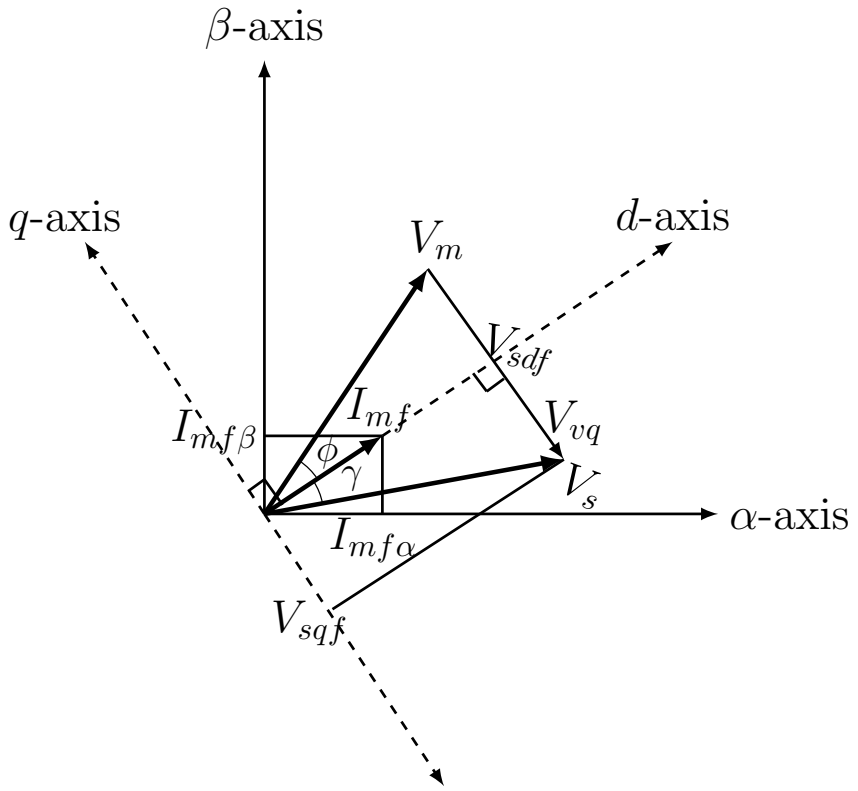

Figure 2.15: Phasor diagram showing the orientation of d-q axes, fundamental component of motor current (I_{mf}) and CSI terminal voltage (V_s).

q-axis controller

The lead angle (γ) at the CSI terminal is ensured by the q-axis controller of the VSI by generating sufficient q-axis component of the VSI voltage (V_{vq}). The resultant of q-axis component (V_{vq}) and the motor voltage (V_m) is the CSI terminal voltage V_s as shown in Figure 2.15. In this Figure the d-axis component of the VSI voltage (V_{vd}) is neglected as its value is very small compared to that of V_{vq}, since the VSI is meant only for reactive power compensation. The VSI however requires a very small active component (V_{vd}) to meet the losses in the inverter and the capacitor. Since the VSI has to maintain the ratio of V_{sdf} and V_{sqf} as in Equation 2.26, the reference to the q-axis controller (V_{sqref}) can be determined using the Equation 2.27.

$$V_{sqref} = -tan(\gamma) * V_{sdf} \tag{2.27}$$

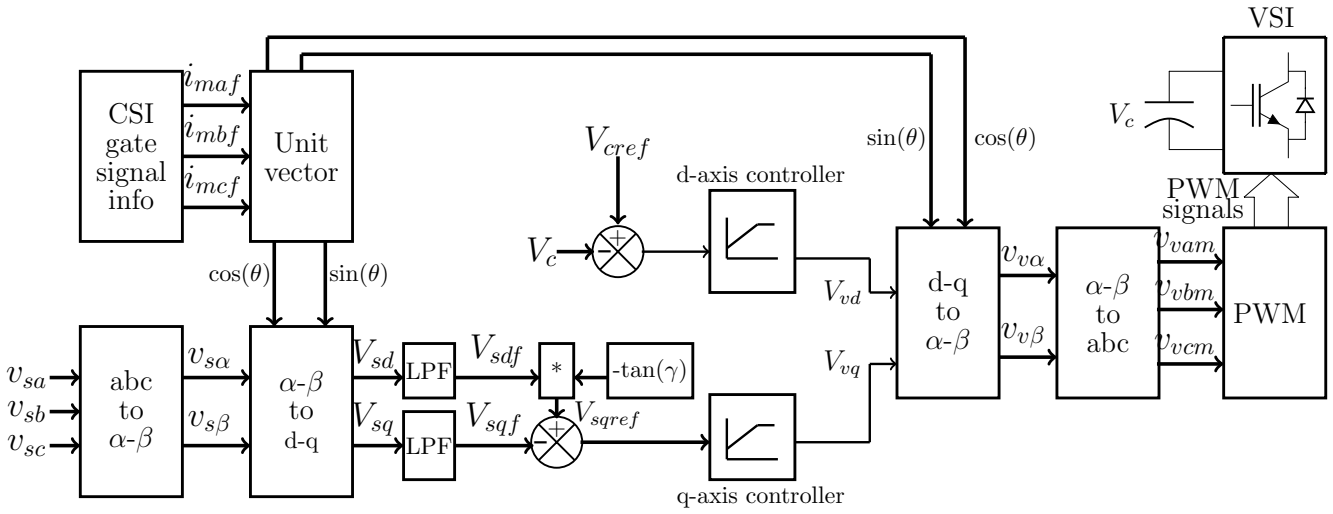

Figure 2.16: Control scheme of VSI

d-axis controller

Since the VSI is controlled to supply only the reactive power to the system, a pre-charged capacitor is sufficient to hold its DC link voltage. The VSI can supply the required reactive power only if its capacitor(C) voltage is maintained at the required minimum level. The power losses in the inverter and capacitor will result in reduction in the capacitor voltage. Hence, a closed loop control is required for balancing of the capacitor voltage. The d-axis PI controller shown in Figure 2.16 is employed for this purpose.

It generates sufficient 'V_{vd}' value to ensure that adequate active power is drawn by the VSI to meet the losses in the inverter and capacitor, so that the capacitor voltage (V_c) is maintained at the reference value (V_{cref}).

The outputs of the controllers along d-axis and q-axis (V_{vd} and V_{vq}) is first transformed to the stationary ($\alpha - \beta$) reference frame to obtain '$v_{v\alpha}$' and '$v_{v\beta}$'. The three phase modulating signals v_{vam}, v_{vbm} and v_{vcm} for the VSI is obtained by the $\alpha - \beta$ to abc transformation. The VSI is operated using the sinusoidal pulse width modulation (SPWM) technique. The gating pulse for the IGBTs is obtained by comparing the three phase modulating voltages (v_{vam}, v_{vbm} and v_{vcm}) with a triangular wave. The implementation of the overall control scheme is depicted in Figure 2.17.

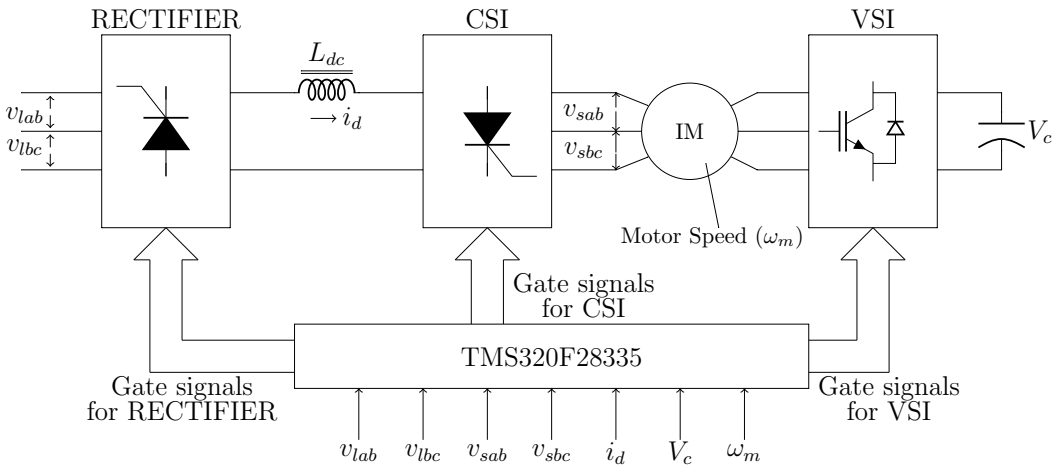

Figure 2.17: Implementation of the overall control scheme of the proposed drive system.

Pre-charging of the VSI capacitor

At starting of the drive the VSI capacitor voltage would be zero hence a control strategy is required to pre-charge the capacitor. The proposed scheme does not require a separate circuit for that, instead the capacitor can be pre-charged by simply turning ON the upper SCR in any one leg and the lower SCR in another leg of the CSI. The capacitor will be charged by the controlled DC current through the turned ON SCRs and the reverse diodes in the IGBTs of the corresponding legs of the VSI as depicted in Figure 2.18. The operation of the control scheme begins once the pre-charging process is completed. The capacitance value (C) can be decided based on the Equation 2.28.

$$C = \frac{i_d(rated)}{F_s \cdot \Delta V} \tag{2.28}$$

where,

$i_d(rated)$ is the rated DC link current, F_s is the switching frequency of the VSI, and ΔV is the allowable ripple voltage in the capacitor.

2.5 Experimental verification

The proposed scheme has been experimentally verified on a 1.5 hP, 415 V, 50 Hz three phase induction motor with open-end stator windings. The motor parameters are shown

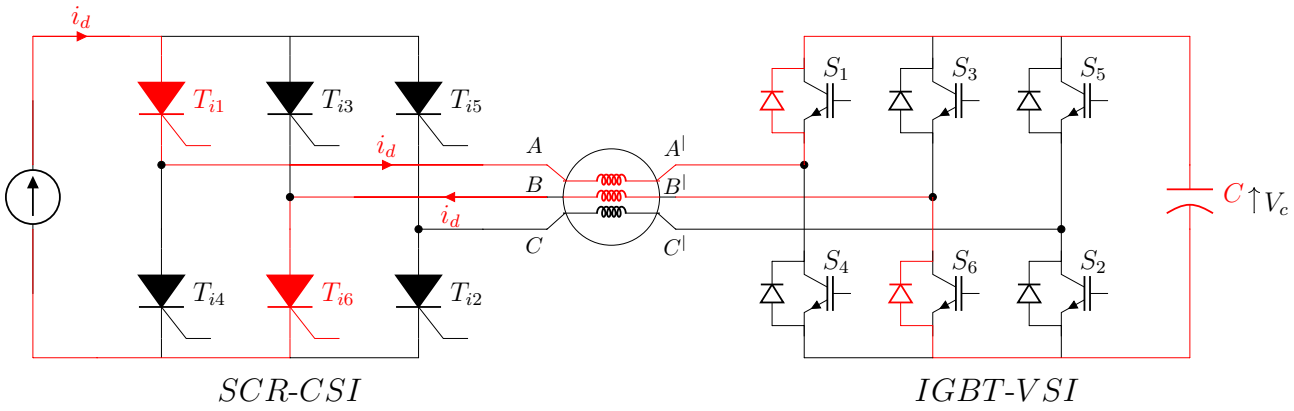

Figure 2.18: Pre-charging scheme of the VSI capacitor

Table 2.2
Induction Motor Parameters

Parameter	Value
No of poles (P)	4
Inertia (J)	0.01 $Kg.m^2$
Stator Resistance (R_s)	8.89 Ω
Rotor Resistance (R_r)	5.51 Ω
Stator inductance (L_s)	24.36 mH
Rotor inductance (L_r)	24.36 mH
Magnetising inductance (L_m)	450.46 mH

in Table.2.2. A DC-link inductor of 200 mH is used to smoothen the output current of the controlled rectifier i_d. Hall effect based voltage and current sensors are used to sense the AC line voltages, DC link current, CSI terminal voltages and the VSI capacitor voltage. Rectifier and current source inverter are built using converter grade SCRs of 1200V and 27A rating. The VSI is built using IGBTs of 1200V, 75A rating and an electrolytic DC link capacitor of 2200µF. It is operated at a switching frequency of 1 kHz. Photograph of the experimental set-up is shown in Figure 2.19.

2.5.1 Steady state performance of the drive

Experimental results depicting the steady state performance of the drive are shown in Figures 2.20 to 2.25. The waveforms of the DC-link current, stator voltage, motor current and the VSI capacitor voltage are shown in these figures for motor operation at different speeds with and without load. It can be seen that the capacitor voltage is constant in all experimental results indicating that the VSI is supplying only reactive power to the

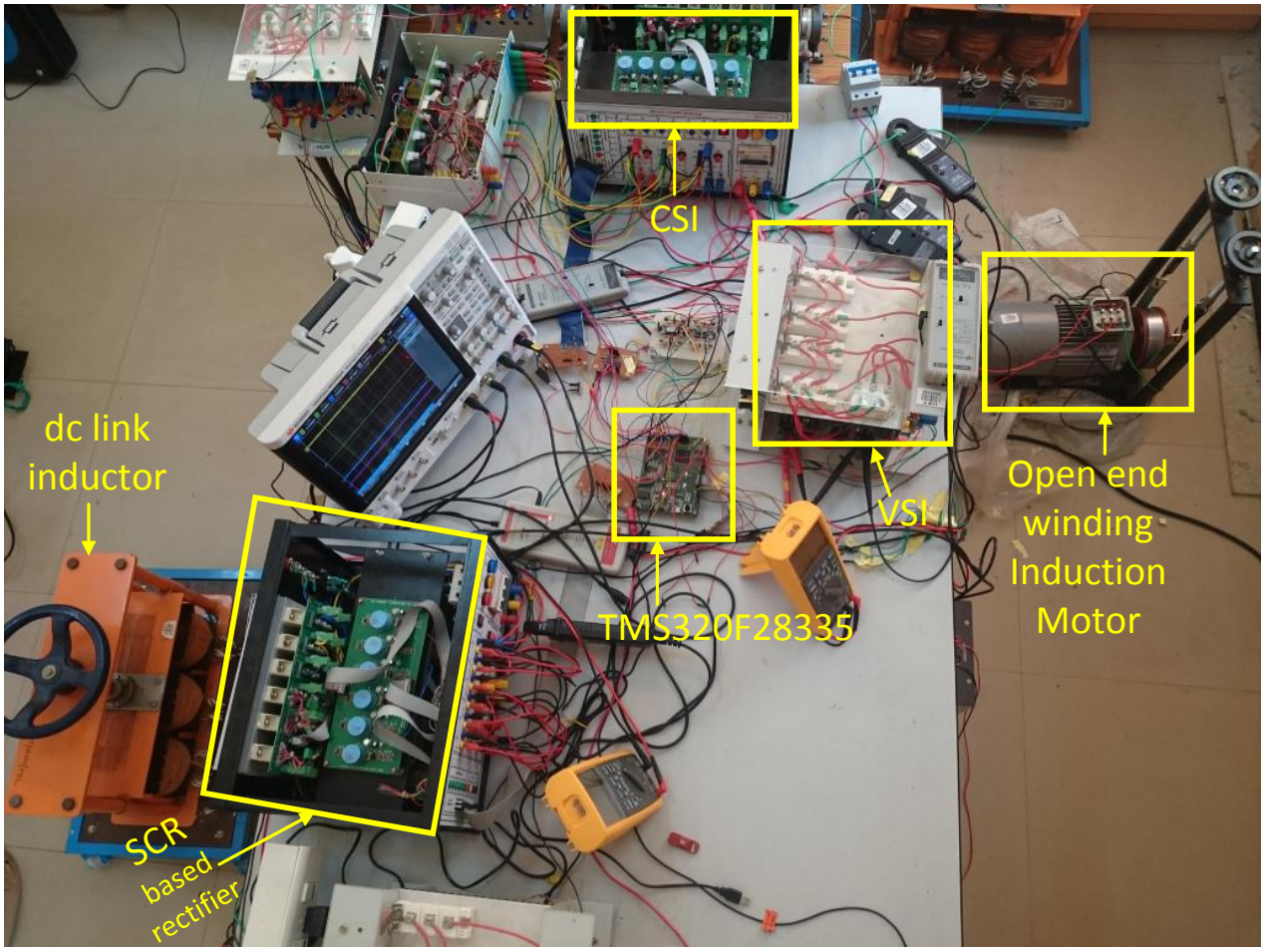

Figure 2.19: Photograph of the experimental setup

system.

2.5.2 Transient performance of the drive

The acceleration of the drive from 300 RPM to 1000 RPM is shown in Figure 2.26. It can be observed that the capacitor voltage is constant during the period of acceleration, proving the effectiveness of the capacitor voltage control scheme in transient conditions also. The response of the drive for step change in speed reference is shown in Figure 2.27.

2.5.3 Low speed operation of the drive

One of the major drawbacks of conventional load commutated CSI-fed drive is the commutation failure during low speed operation, due to insufficient motor back EMF. While

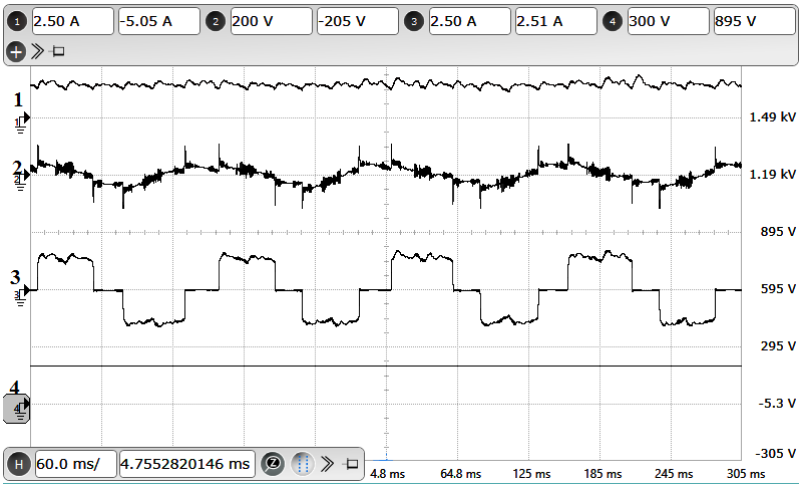

Figure 2.20: Experimental results: Motor operation at 200 RPM : X-axis: 60 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 200 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

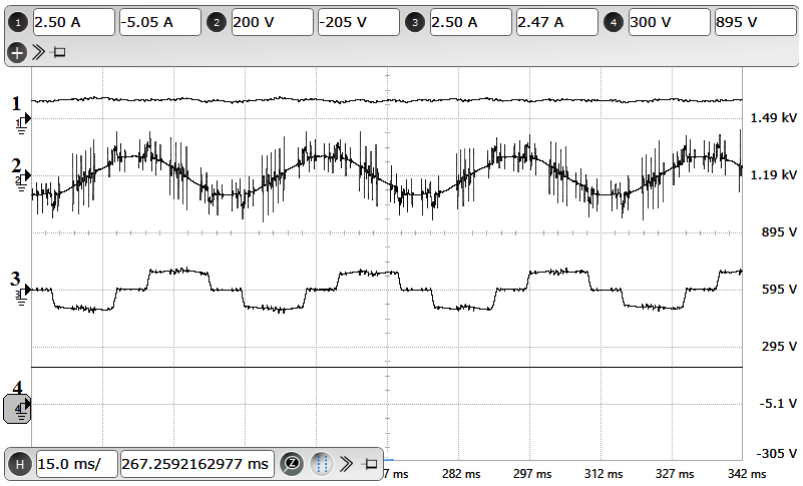

Figure 2.21: Experimental results: Motor operation at 750 RPM : X-axis: 15 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 200 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

most of the CSI-VSI hybrid systems cited in this thesis need a separate scheme to run the drive at startup and low speeds, the proposed system is free from such deficiency since the VSI can facilitate load commutation of the SCRs under all conditions. In the load commutated ARIM structure presented in Chapter-1, the capability of the drive to deliver starting torque is limited as the motor would be started using the VSI connected to the low voltage excitation winding of the ARIM. In the proposed system the induction motor can be operated at low speeds, delivering the rated torque without the problem of com-

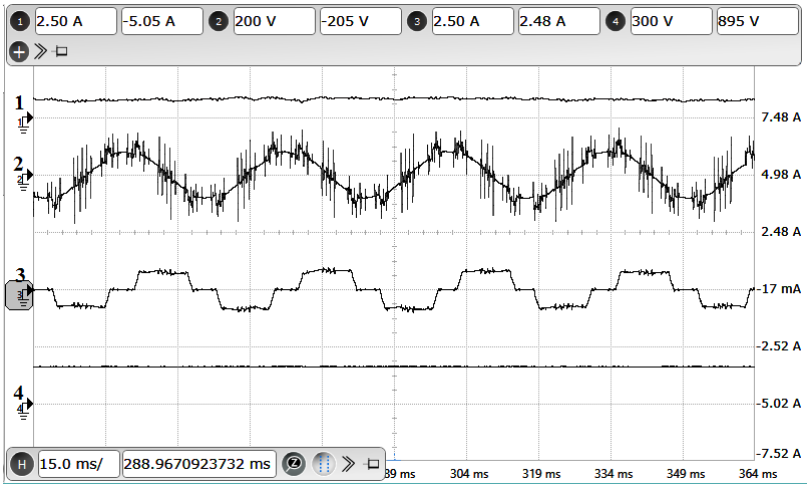

Figure 2.22: Experimental results: Motor operation at 900 RPM : X-axis: 15 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 200 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

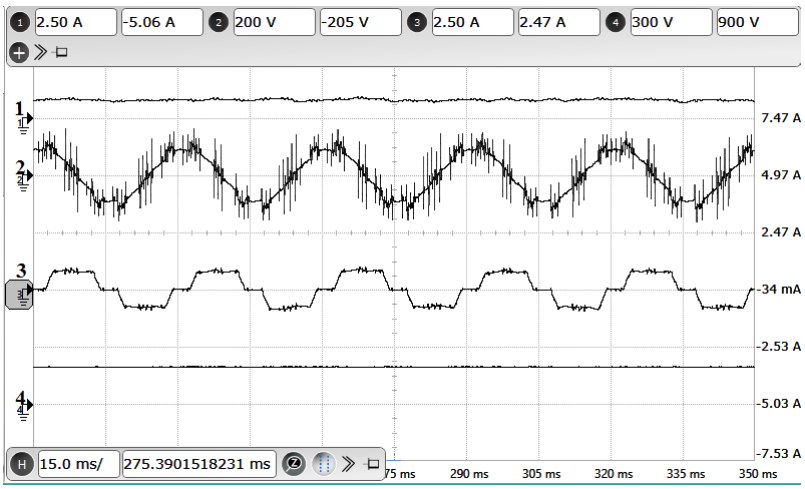

Figure 2.23: Experimental results: Motor operation at 1000 RPM : X-axis: 15 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 200 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

mutation failure. The steady state waveforms of the drive during low speed operation in the range from 50 RPM to 100 RPM are shown in Figures from 2.28 to 2.30. The experimental verification of the proposed scheme is carried out on a 10 HP induction motor also and the results are given in appendix A-3.

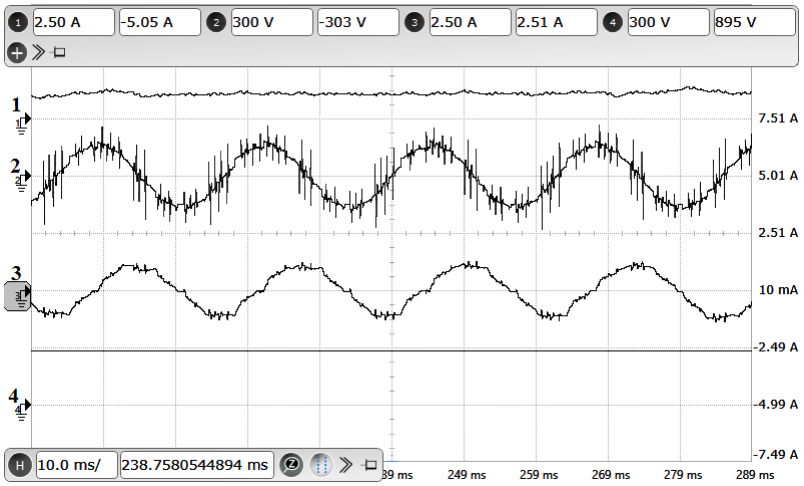

Figure 2.24: Experimental results: Motor operation at 1300 RPM : X-axis: 10 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 300 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

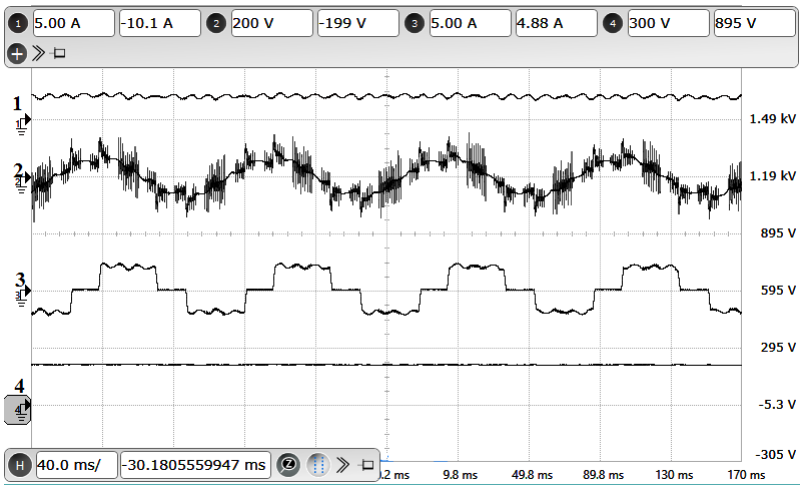

Figure 2.25: Experimental results: Motor operation at 300 RPM in loaded condition : X-axis: 40 ms/div. Ch-1: DC link current (Y-axis: 5 A/div). Ch-2: A-phase stator voltage(Y-axis: 200 V/div). Ch-3: A-phase motor current (Y-axis: 5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

2.6 Converter ratings

The ratings of the CSI and the VSI are decided mainly based on the motor power rating. In the proposed load commutated drive the CSI would supply the real power requirement of the motor while the VSI would meet the reactive power requirement of the motor as well as the additional reactive power required to maintain the lead angle between the motor current and the CSI terminal voltage for ensuring load commutation of the SCRs. The

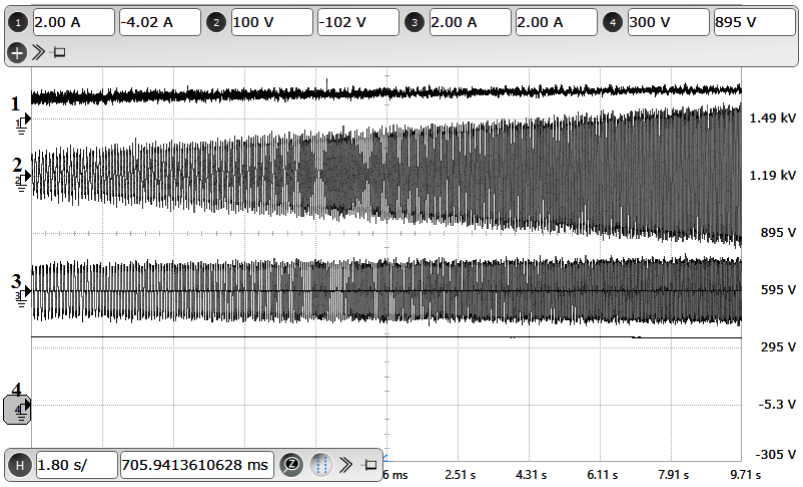

Figure 2.26: Experimental results: Motor accelerated from 300 RPM to 1000 RPM : X-axis: 1.8 s/div. Ch-1: DC link current (Y-axis: 2 A/div). Ch-2: A-phase stator voltage(Y-axis: 100 V/div). Ch-3: A-phase motor current (Y-axis: 2 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

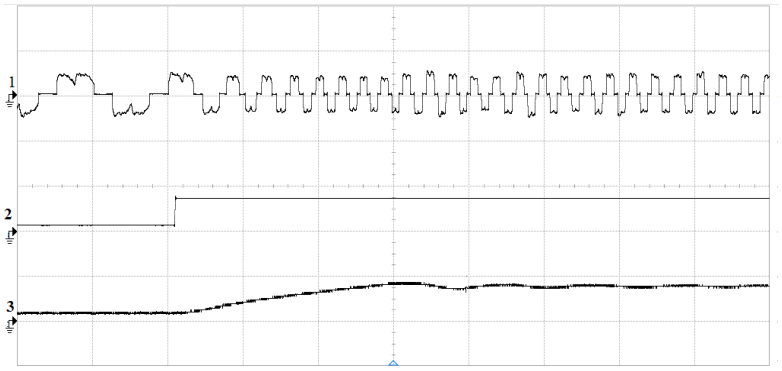

Figure 2.27: Experimental results: Step change in motor speed from 100 RPM to 500 RPM: X-axis: 200 ms/div. Ch-1: A-phase motor current (Y-axis: 2 A/div). Ch-2: Motor speed reference (Y-axis: 666 rpm/div). Ch-3: Actual motor speed (Y-axis: 666 rpm/div).

current rating of the CSI and the VSI is same as the motor current rating, as they are connected in a series configuration. However the voltage ratings of the converters are different. The terminal voltage of the CSI will be the vector sum of the voltage appearing across the motor windings and the voltage of the VSI. This is evident from the system phasor diagram depicting CSI terminal voltage (V_s), motor voltage (V_m), and VSI voltage (V_v) shown in Figure 2.10. As the VSI is used only for supplying the reactive power required to maintain leading power factor at the CSI terminals the voltage rating of the VSI can be found from the reactive power requirement of the system, considering the motor voltage, motor power factor angle (ϕ) and lead angle (γ).

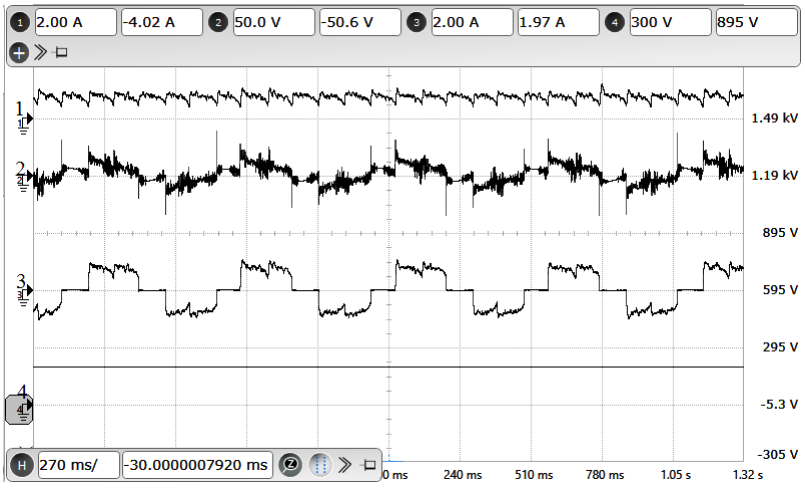

Figure 2.28: Experimental results: Motor operation at 50 RPM : X-axis: 270 ms/div. Ch-1: DC link current (Y-axis: 2 A/div). Ch-2: A-phase stator voltage(Y-axis: 50 V/div). Ch-3: A-phase motor current (Y-axis: 2 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

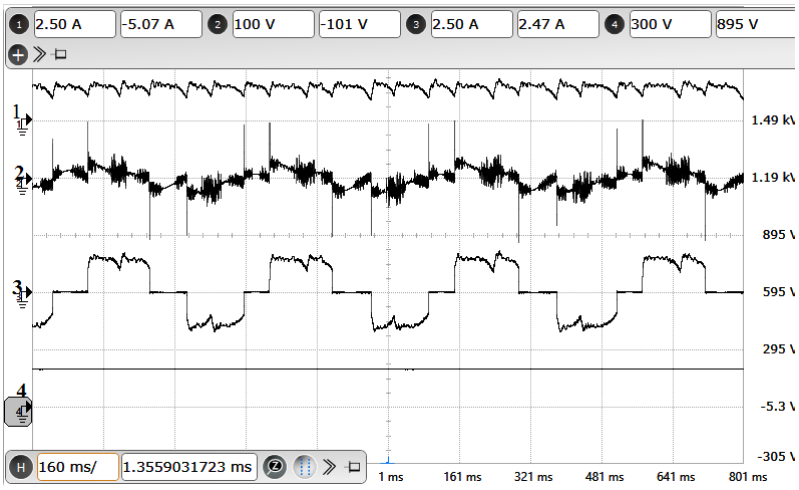

Figure 2.29: Experimental results: Motor operation at 70 RPM : X-axis: 160 ms/div. Ch-1: DC link current (Y-axis: 2.5 A/div). Ch-2: A-phase stator voltage(Y-axis: 100 V/div). Ch-3: A-phase motor current (Y-axis: 2.5 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

The angle γ which corresponds to the turn OFF time of SCR would be small if the CSI is built using fast turn OFF inverter grade SCRs, and hence this angle is neglected while arriving at the converter rating. The active power requirement of the motor would be proportional to $V_m cos(\phi)$, where ϕ is the motor power factor angle. In addition to the active power required by the motor the CSI would also supply a small amount of active power to the VSI for meeting the losses in the capacitor and the IGBTs in order to maintain the voltage across the capacitor at a constant value. Since the active power

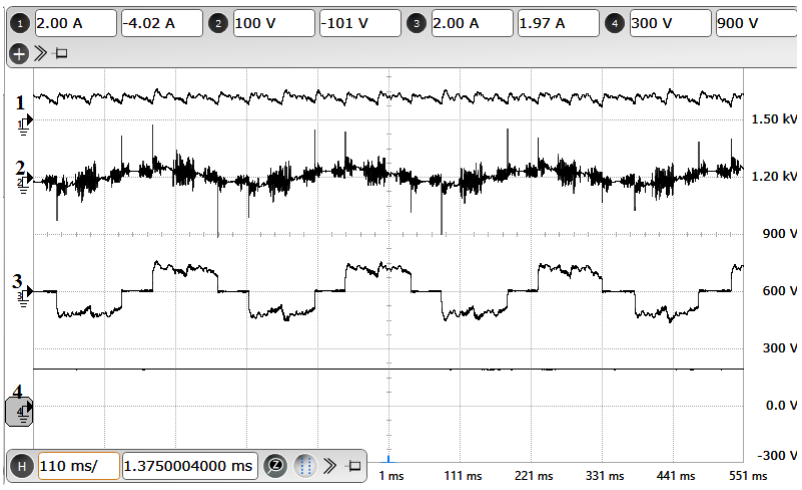

Figure 2.30: Experimental results: Motor operation at 100 RPM : X-axis: 110 ms/div. Ch-1: DC link current (Y-axis: 2 A/div). Ch-2: A-phase stator voltage(Y-axis: 100 V/div). Ch-3: A-phase motor current (Y-axis: 2 A/div). Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

supplied by the CSI to the VSI is very small compared to that supplied to the motor, it can be neglected while arriving at the voltage rating of the CSI. Hence the voltage rating of the CSI is given by:

$$V_s = V_m \cdot cos(\phi) \tag{2.29}$$

Similarly the reactive power component of the motor is $V_m sin(\phi)$ which would be supplied by the VSI. Hence the voltage rating of the VSI is given by:

$$V_v = V_m \cdot sin(\phi) \tag{2.30}$$

In high power machines, with the ratio of the apparent power (kVA), active power, and reactive power is approximately equal to 1:0.9:0.2.

Hence in the proposed drive system the approximate CSI voltage rating (V_s) in per unit is 0.9 p.u and the VSI voltage rating (V_v) would be 0.2 p.u.

2.7 Conclusion

A new scheme for a SCR-based load-commutated CSI fed induction motor drive with open-end stator winding is presented in this chapter. The proposed scheme uses a capacitor fed VSI connected at one end of the stator winding to make the power factor leading at the terminals of the CSI connected at the other end of the stator windings. Since the CSI current leads ahead of the CSI terminal voltage under all conditions of operation of the motor, the SCRs of the CSI are naturally commutated. The CSI supplies the entire active power required by the motor. The VSI on the other hand supplies only the reactive power required to maintain slightly leading power factor at the CSI terminals and hence the power handled by the VSI is only 20-25$\%$ of that of the CSI, in high power motors. The CSI is switched at fundamental frequency and hence the switching losses are considerably lesser compared to that of pulse width modulated inverters. This reduction in switching loss is significant in high power applications. The experimental results demonstrated the ability of the proposed drive scheme to operate at very low speed without any external commutation circuit. This is a significant advantage compared to the CSI-fed synchronous motor drives which experience commutation failure at low speed due to insufficient back EMF. Since induction motors are more rugged, reliable, efficient, and cheaper than synchronous motors, the proposed scheme has the potential to be considered for high power applications where load-commutated CSI-fed synchronous motor drives are in use at present. The proposed drive scheme is experimentally verified on 1.5 HP and 10 HP induction motors with open-end stator windings, under transient as well as steady state operating conditions. However the motor current in this scheme is quasi square wave in shape which contains significant amount of 5^{th} and 7^{th} harmonics that can lead to 6^{th} harmonic torque pulsations in the drive. This issue is addressed in the multilevel current source inverter fed load commutated induction motor drive proposed in the next chapter.

Chapter 3

Load Commutated Multilevel Current Source Inverter fed Open-end Winding Induction Motor Drive

3.1 Introduction

In the scheme proposed in Chapter-2 the motor current is quasi square wave in nature because the CSI operates in 120 degrees conduction mode. This results in high content of 5^{th} and 7^{th} harmonics in the motor current, and it is a well established fact that these harmonics can cause 6^{th} harmonic torque pulsations in the motor. This chapter proposes a load commutated multilevel current source inverter configuration to improve the quality of the motor current so as to reduce the torque pulsations in the motor. Additionally, the multilevel configuration can reduce the device (SCR) current rating and also would improve the reliability of the system by bringing in redundancy [32, 72, 73] in the system. A multilevel CSI configuration for IM drive consisting of two different current source inverters, a load commutated SCR based CSI and a GTO based CSI is presented in [74]. This configuration was a replacement for GTO based multilevel CSI presented in [75]. But GTO based topologies suffer from a major disadvantage that their gate driver circuit design is complex due to the high negative gate current requirement for commutation of the GTOs. The proposed scheme uses only SCRs for realizing multilevel load commutated CSI structure for induction motor drives.

The block diagram of the proposed scheme is shown in Figure 3.1. It consists of a SCR based multilevel CSI connected to one end of the stator winding to meet the real power requirement of the system, while the other end of the stator winding is directly interfaced with a capacitor-fed IGBT based VSI for reactive power compensation and also to facilitate load commutation of the SCRs. The multilevel CSI structure is realized using two two-level current source inverters operated with a phase shift of 30 degrees.

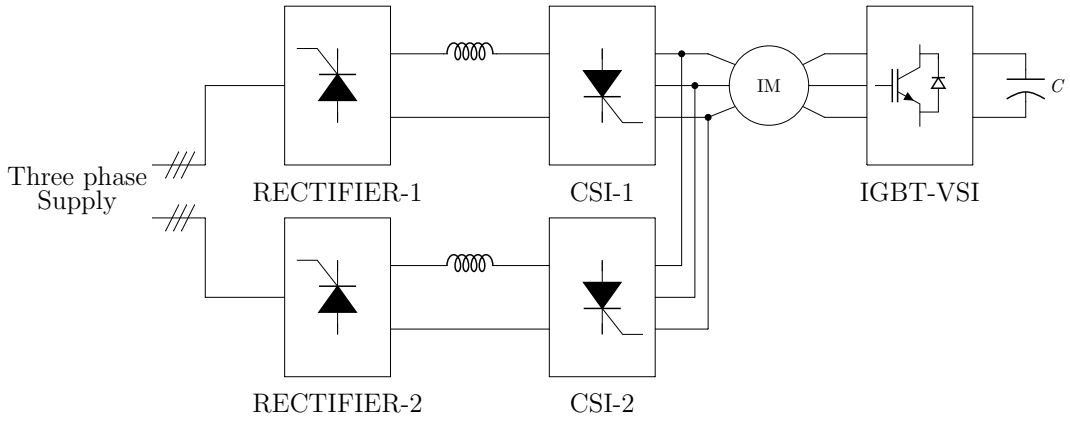

Figure 3.1: Block diagram of the proposed load commutated multilevel CSI scheme for open-end winding induction motor drives.

3.2 Analysis of the phase-shifted operation of two CSIs

In this section a mathematical analysis of the amount of the phase shift required to be maintained between the two CSIs for attaining minimum 5^{th} and 7^{th} harmonics in the motor current is presented. From the block diagram shown in Figure 3.1 it can be observed that the current through the motor winding would be the resultant of the individual CSI (CSI-1 and CSI-2) currents. The phase shifted operation of the two CSIs will result in a current waveform with multilevel profile in the motor windings. Figure 3.2 shows the individual quasi square wave currents of CSI-1 and CSI-2 with the magnitudes equal to the respective DC-link currents ($\frac{i_d}{2}$), and the resultant multilevel motor current waveform. In Figure 3.2 the phase shift between the two CSI currents is denoted as 'δ' degrees. The CSI-2 current waveform lags behind the CSI-1 current waveform by angle 'δ'. A harmonic analysis of the multilevel motor current waveform can be carried out using Fourier series.

The generalized Fourier series expansion of a periodic waveform $f(t)$ with time period T is given as:

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n cos(n\omega t) + \sum_{n=1}^{\infty} b_n sin(n\omega t) \tag{3.1}$$

where n = 1,2,3..., is an integer that denotes the n^{th} frequency component.
The Fourier coefficients a_0, a_n, b_n can be obtained using the following expressions:

$$a_0 = \frac{1}{T}\int_0^T f(t)dt \tag{3.2}$$

$$a_n = \frac{2}{T}\int_0^T f(t)cos(n\omega t)dt \tag{3.3}$$

$$b_n = \frac{2}{T}\int_0^T f(t)sin(n\omega t)dt \tag{3.4}$$

The multilevel motor current waveform shown in Figure 3.2 has odd symmetry and its average value is zero. Hence the Fourier series coefficients:
a_0=0
a_n=0

$$b_n = \frac{2}{T}\int_0^T f(t)sin(n\omega t)dt \tag{3.5}$$

From Figure 3.2 it can be observed that the multilevel motor current waveform exhibits half wave symmetry and quarter wave symmetry. The current levels in this waveform are $+i_d$, $+\frac{i_d}{2}$, 0, $-\frac{i_d}{2}$, $-i_d$. It can be noted that the duration of the current level $+\frac{i_d}{2}$ (and also $-\frac{i_d}{2}$) is dependent on the phase shift angle 'δ'.

Since the multilevel current waveform exhibits quarter wave symmetry, the Fourier coefficient b_n shown in Equation 3.5 can be re-written as Equation 3.6,

$$b_n = \frac{8}{T}\int_0^{\frac{T}{4}} f(t)sin(n\omega t)dt \tag{3.6}$$

Using the above equation, the Fourier coefficient b_n of the multilevel current wave-

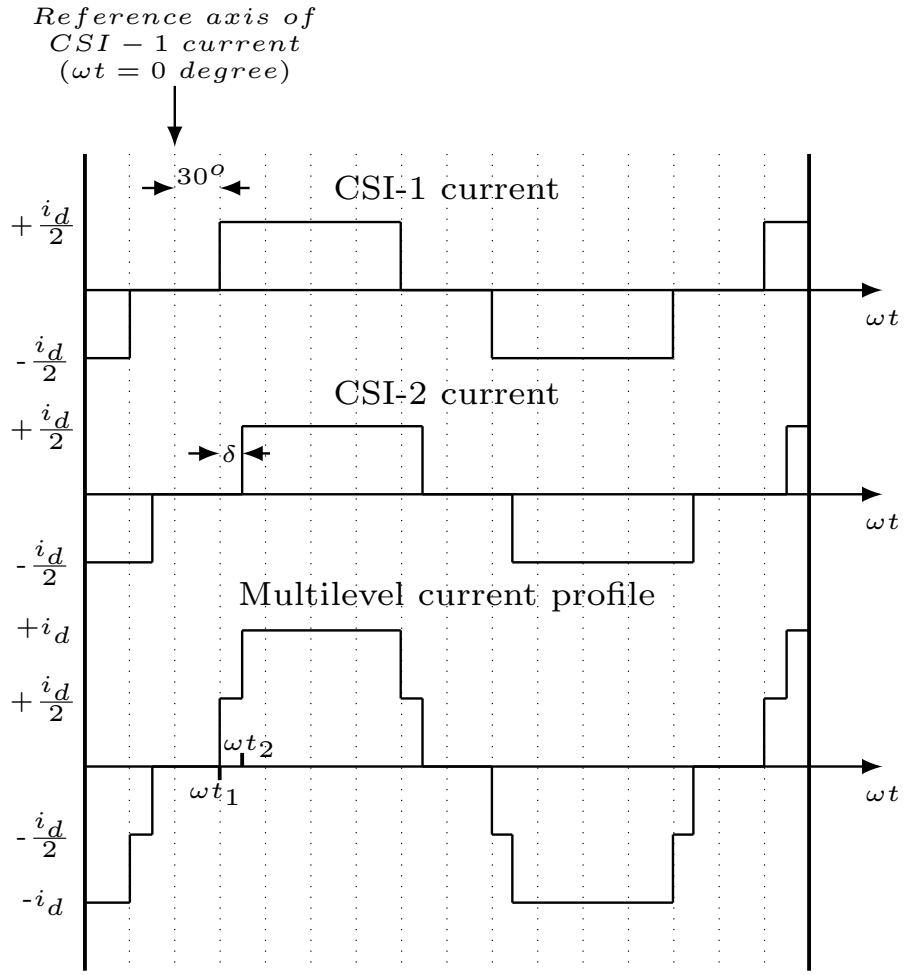

Figure 3.2: Multilevel current waveform with δ angle phase shifted operation of CSIs.

form as a function of phase shift angle 'δ' can be expressed as follows:

$$b_n = \frac{4}{\pi}[\int_{30-\frac{\delta}{2}}^{30+\frac{\delta}{2}} \frac{i_d}{2} \cdot sin(n\omega t)d(\omega t) + \int_{30+\frac{\delta}{2}}^{\frac{\pi}{2}} i_d \cdot sin(n\omega t)d(\omega t)] \tag{3.7}$$

On further simplification b_n can be written as,

$$b_n = \frac{4}{n\pi} \cdot i_d[cos(n \cdot (30 + \frac{\delta}{2}) + cos(n \cdot (30 - \frac{\delta}{2})] \tag{3.8}$$

Now, by substituting the values for n = 1, 5 and 7, the Fourier coefficients of the fundamental component (b_1), 5^{th} harmonic component (b_5), 7^{th} harmonic component (b_7) can be obtained as below:

$$b_1 = \frac{4}{\pi} \cdot i_d[cos(30 + \frac{\delta}{2})) + cos(30 - \frac{\delta}{2})] \tag{3.9}$$

$$b_5 = \frac{4}{5\pi} \cdot i_d[cos(5 \cdot (30 + \frac{\delta}{2})) + cos(5 \cdot (30 - \frac{\delta}{2}))] \tag{3.10}$$

$$b_7 = \frac{4}{7\pi} \cdot i_d[cos(7 \cdot (30 + \frac{\delta}{2})) + cos(7 \cdot (30 - \frac{\delta}{2}))] \tag{3.11}$$

The Fourier coefficients b_1, b_5, b_7 shown in Equations (3.9), (3.10), (3.11) are used to plot the variation of 5^{th} and 7^{th} harmonic contents in the multilevel motor current waveform with respect to the phase shift angle 'δ'. The range of variation in phase shift angle δ will have the following constraint as in Equation (3.12), so that the symmetry of multilevel current waveform remains intact.

$$0 < \delta < 60^{\circ} \tag{3.12}$$

The 5^{th} and 7^{th} harmonic components relative to the fundamental component can be expressed as,

$$\frac{b_5}{b_1} = \frac{\frac{4}{5\pi} \cdot i_d[cos(5 \cdot (30 + \frac{\delta}{2})) + cos(5 \cdot (30 - \frac{\delta}{2}))]}{\frac{4}{\pi} \cdot i_d[cos(30 + \frac{\delta}{2}) + cos(30 - \frac{\delta}{2})]} \tag{3.13}$$

$$\frac{b_7}{b_1} = \frac{\frac{4}{7\pi} \cdot i_d[cos(7 \cdot (30 + \frac{\delta}{2})) + cos(7 \cdot (30 - \frac{\delta}{2}))]}{\frac{4}{\pi} \cdot i_d[cos(30 + \frac{\delta}{2}) + cos(30 - \frac{\delta}{2})]} \tag{3.14}$$

Considering only the 5^{th} and 7^{th} harmonics the total harmonic distortion (THD) of the motor current can be calculated as given in Equation 3.15

$$THD = \frac{\sqrt{b_5^2 + b_7^2}}{b_1} \tag{3.15}$$

The variation in THD, 5^{th} harmonic and 7^{th} harmonic with phase shift angle (δ) is shown in Fig.3.3.

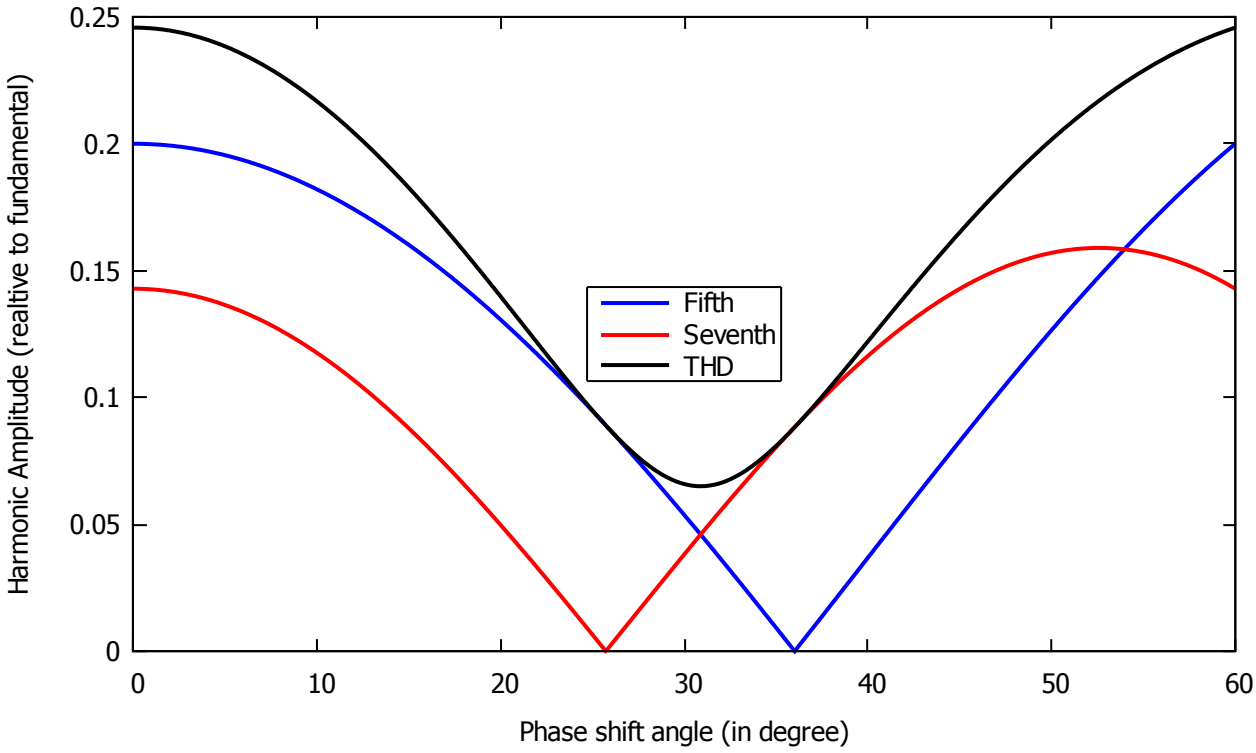

Figure 3.3: Variation in 5^{th} harmonic , 7^{th} harmonic and the THD of motor current with respect to the phase shift angle δ between the output currents of CSI-1 and CSI-2.

When the phase shift angle δ=0° the motor current waveform will be a quasi square waveform whose 5^{th} and 7^{th} harmonic contents are 20% and 14% of the fundamental respectively as seen in Figure 3.3. With, δ=30° the THD (accounting only 5^{th} and 7^{th} harmonics), is the minimum, with 5^{th} and 7^{th} harmonic contents as 5.38% and 3.86% respectively. Hence δ=30° is the optimal phase shift angle to be maintained between the output currents of CSI-1 and CSI-2 to achieve minimum THD in the motor current with corresponding low values of 5^{th} and 7^{th} harmonics. It can be seen from Table 3.1 that 5^{th} harmonic can be eliminated if δ=26° and 7^{th} harmonic can be eliminated if δ=36°.

Table 3.1
5^{th} and 7^{th} harmonic present in the multilevel motor current for different values of the phase shift angle (δ)

δ angle(in degrees)	5^{th} harmonic content (relative to fundamental in $\%$)	7^{th} harmonic content (relative to fundamental in $\%$)
δ= 0°	20$\%$	14.28$\%$
δ= 26°	9$\%$	0$\%$
δ=30°	5.36$\%$	3.83$\%$
δ=36°	0$\%$	8$\%$

3.3 Power circuit description of multilevel CSI fed IM drive

Complete power circuit diagram of the proposed load commutated multilevel CSI scheme for open-end winding induction motor is shown in Figure 3.4. The current sources at the input side are built using SCR based controlled rectifiers in series with large DC-link inductors (L_{dc}). The multilevel CSI is realized using two SCR based current source inverters, CSI-1 and CSI-2 connected in parallel configuration but operated with a phase shift of 30°. This parallel combination of the two current source inverters are connected to one end of the stator windings of the induction motor, while the other end is connected to an IGBT based voltage source inverter. Both CSI-1 and CSI-2 are operated in 120 degrees mode of conduction resulting in quasi square wave output current in each inverter, as shown in Figure 3.5. However, since these two CSIs are operated with a phase shift of 30° the current flowing through the motor winding will have a multilevel profile as shown in Figure 3.5. As discussed in the previous section, the 5^{th} and 7^{th} harmonic contents in the motor current would be 5.36% and 3.83% (relative to fundamental) respectively, as against 20% of 5^{th} harmonic and 14.35% of 7^{th} harmonic present in the quasi-square current of traditional load commutated CSI fed drive [76],[77]. This drastic reduction in 5^{th} and 7^{th} harmonic content would reduce the harmonic losses and torque pulsations experienced by the motor. Even though stepped current flows through the motor winding, motor voltage would be almost sinusoidal in nature. The load commutation of SCR based multilevel CSI necessitates leading power factor operation of both CSI-1 and CSI-2. Various sub-circuits of the multilevel CSI fed drive are discussed in detail in the following sections.

3.3.1 Line commutated rectifiers

Two SCR based line commutated rectifiers (Rectifier-1 and Rectifier-2 shown in Figure 3.4) are used to build two current sources for feeding the CSIs. These rectifiers are fed from two isolated three phase AC supplies to avoid any circulating current. The SCRs of Rectifier-1 (T_{ru1} to T_{ru6}) and Rectifier-2 (T_{rl1} to T_{rl6}) are triggered independently at firing angles α_1 and α_2 respectively to maintain the individual DC-link currents (i_{d1} and i_{d2}) at the required reference values. The gating pulses of the SCRs of Rectifier-1 (G_{Tru1} to G_{Tru6}) and Rectifier-2 (G_{Trl1} to G_{Trl6}) are generated in synchronism with the sensed input AC supply, as described in the Chapter-2 of this thesis.

3.3.2 Multilevel CSI

Multilevel CSI consists of two current source inverters CSI-1 and CSI-2 connected in parallel configuration as shown in Figure 3.4. Both CSI-1 and CSI-2 are connected to the stator terminals (A-B-C) of the open-end winding IM. The CSI-1 and CSI-2 currents flowing through the motor windings results in a multilevel current profile owing to the 30° phase shifted operation of the CSIs. The gating pulses of SCRs (T_{iu1} to T_{iu6}) of CSI-1 (G_{Tiu1} to G_{Tiu6}) and the SCRs (T_{il1} to T_{il6}) of CSI-2 (G_{Til1} to G_{Til6}), are shown along with the SCR conduction periods in Figure 3.6. Gating pulse waveforms are drawn taking the fundamental component of the A-phase currents in CSI-1 (i_{s1af}) and CSI-2(i_{s2af}) as the references.

3.3.3 Capacitor fed VSI

The VSI configuration in the proposed multilevel CSI fed drive is similar to that presented in Chapter-2. The VSI is connected to the stator terminals ($A^{|}$, $B^{|}$, $C^{|}$) of the open-end winding IM and it consists of six IGBTs (S_1 to S_6) and a voltage holding capacitor 'C'.

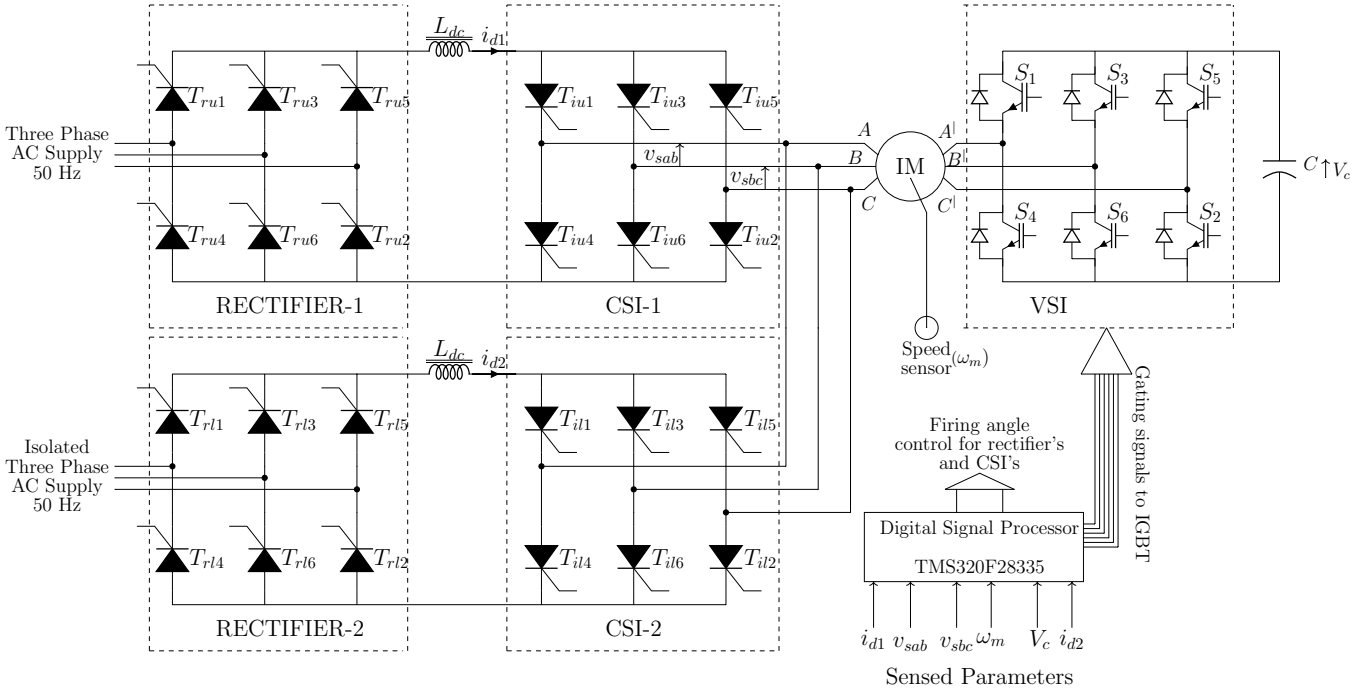

Figure 3.4: Power circuit diagram of the proposed load commutated multilevel CSI scheme for open-end winding induction motor drive.

3.4 Basic principles of load commutation in the proposed multilevel CSI fed IM drive

Figure 3.7 shows the A-phase motor current waveform i_{ma} and its fundamental component i_{maf} that leads ahead of the CSI terminal voltage v_{sa} (A-phase voltage) by angle β. This lead angle β has to be ensured throughout the motor operation for the load commutation of both current source inverters connected to one side of the motor windings. The IGBT based VSI with a voltage holding capacitor 'C', directly interfaced to the other side of the stator winding, is used for reactive power compensation to ensure this lead angle β. Figure 3.8 shows a phasor diagram depicting the CSI terminal voltage (V_s), motor voltage (V_m), VSI output voltage (V_v) and the fundamental components of the motor current (I_{mf}), CSI-1 current (I_{s1f}) and CSI-2 current (I_{s2f}). The phasor (I_{mf}) of the fundamental component of motor current lags behind the motor voltage phasor (V_m) by the power factor angle ϕ. Also, the phasor (I_{s2f}) of the fundamental component of CSI-2 current lags behind that of CSI-1 current (I_{s1f}) by an angle of 30^0, owing to their phase shifted operations. The resultant of I_{s1f} and I_{s2f}, is the motor current phasor (I_{mf}). The oper-

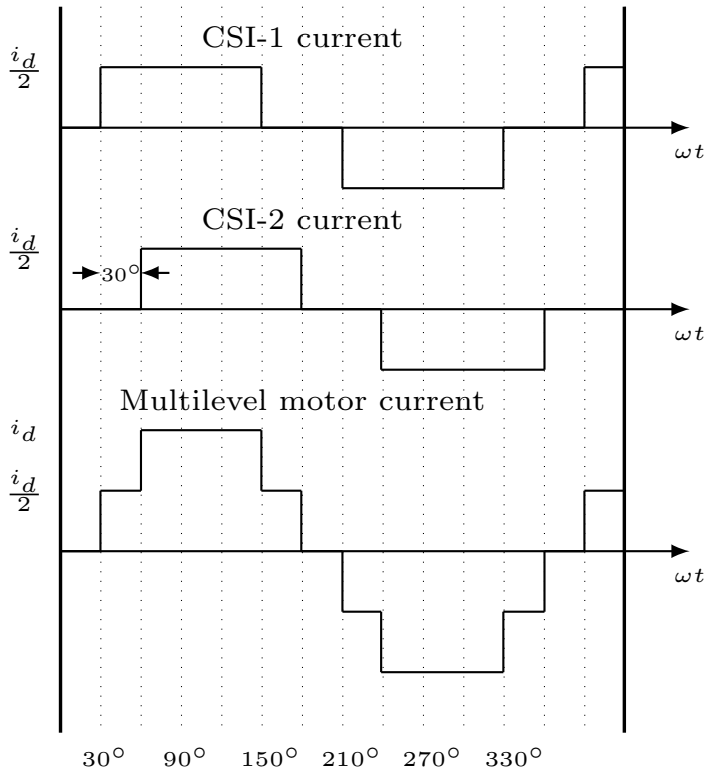

Figure 3.5: Motor current and CSI current waveforms.

ation of VSI is controlled in such a way that it exchanges only reactive power with the system. The CSI terminal voltage phasor (V_s) that lags behind the motor current phasor (I_{mf}) by the angle β is the phasor sum of motor voltage and the VSI voltage (V_v) as given in Equation 3.16.

$$\vec{V_s} = \vec{V_m} + \vec{V_v} \tag{3.16}$$

The lead angle β is decided based on the system requirement, such that it ensures leading power factor operation of both CSI-1 and CSI-2. Figure 3.7 shows the fundamental component of A-phase motor current (i_{maf}) that leads ahead of the A-phase CSI terminal voltage or phase voltage (v_{sa}) by an angle β. The CSI line voltage (v_{sab}) leads ahead of the CSI terminal voltage or phase voltage (v_{sa}) by 30°. Infact, it is the CSI line voltage which would perform the commutation of SCRs of both CSI-1 and CSI-2. In Figure 3.7, A-phase top SCR (T_{iu1}) of CSI-1 is triggered at the instant 't_1' and would be in conduction till 't_3' for a duration of 120 °.

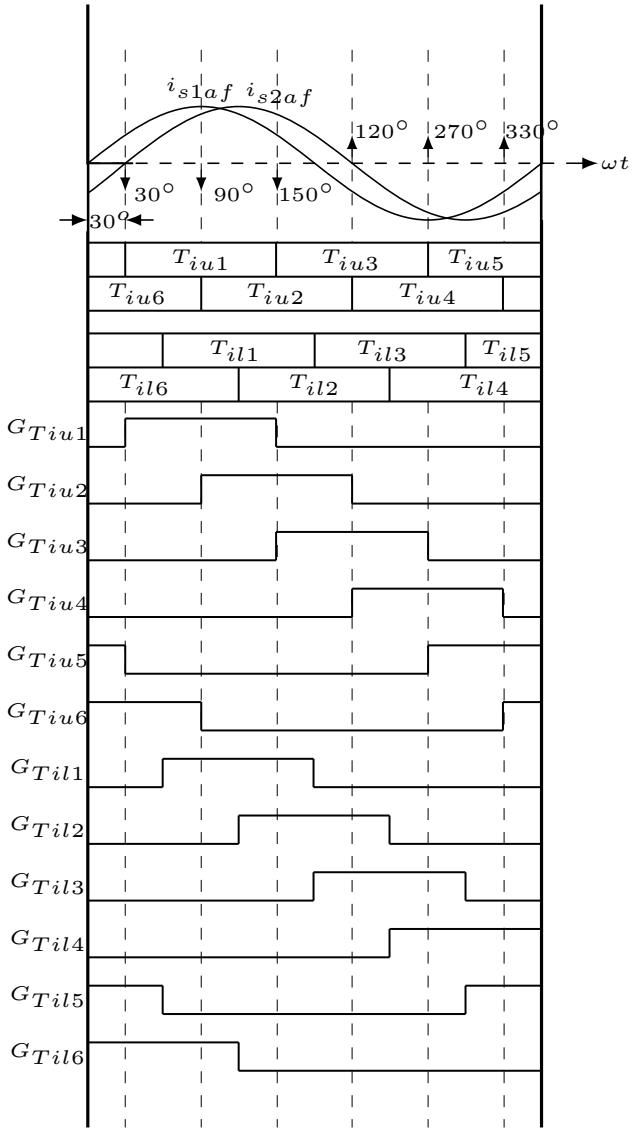

Figure 3.6: SCR conduction period and their gating pulses of CSI-1 and CSI-2.

The A-phase top SCR of CSI-2 (T_{il1}) is triggered at 't_2' and it conducts for a duration of 120° till 't_4'. At the instant 't_3' B-phase top SCR of CSI-1 (T_{iu3}) is triggered and the line voltage v_{sab} will turn OFF the SCR T_{iu1} (since v_{sab} appears as reverse voltage across the SCR T_{iu1}). Similarly, at 't_4' B-phase top SCR of CSI-2 (T_{il3}) is triggered and the same line voltage v_{sab} turns OFF the A-phase top SCR of CSI-2 (T_{il1}). From the instant 't_4', the line voltage v_{sab} should remain positive for a period equivalent to the commutation angle 'γ'. In order to ensure proper commutation, 'γ' should be greater than the turn-OFF time of the SCRs. In the multilevel CSI configuration if the CSI terminal voltage v_{sa} is made to lag behind the fundamental component of the motor current by an angle β=$(15 + \gamma)$

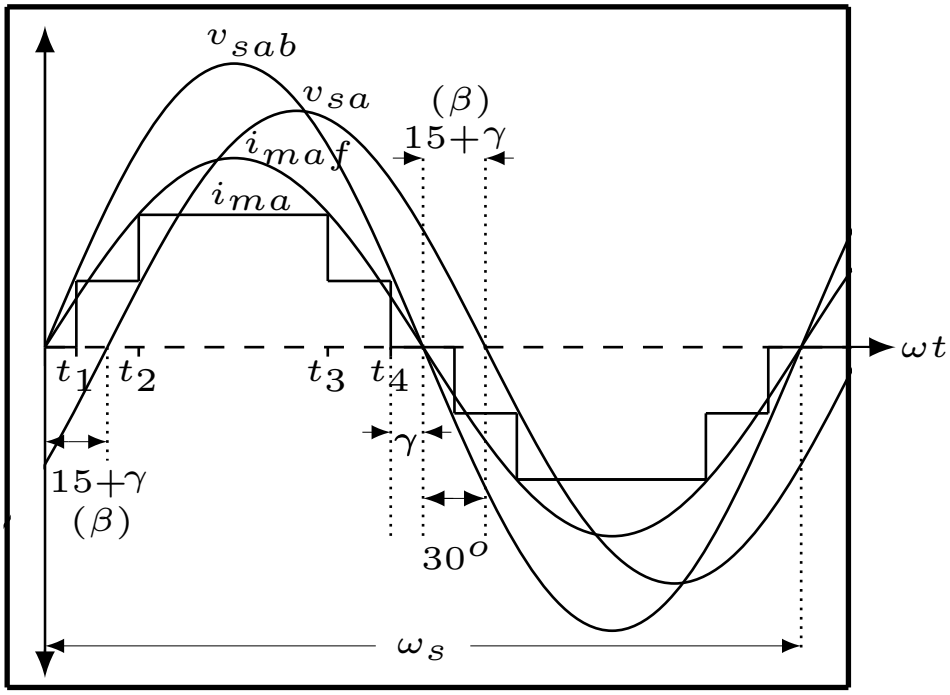

Figure 3.7: Waveforms of CSI line voltage (v_{sab}), CSI terminal voltage (v_{sa}), motor current (i_{ma}) and its fundamental component (i_{maf}) during motoring operation.

degrees, the CSI line voltage v_{sab} will ensure proper turn OFF of A-phase top SCRs of both CSI-1 and CSI-2. In other words to ensure load commutation of the SCRs a lead angle β=$(15 + \gamma)$ should be maintained.

3.5 Control Scheme

The overall control scheme of the proposed system mainly consists of two sections:

- Control scheme of the multilevel CSI for motor speed control.
- Control scheme of the VSI to ensure load commutation.

3.5.1 Control scheme of the multilevel CSI

Speed control of the motor is performed by varying the DC-link currents i_{d1}, i_{d2} (normally i_{d1}= i_{d2} = $\frac{i_d}{2}$) and the CSI frequency. The control scheme of the multilevel CSI is depicted in Figure 3.9. The error in motor reference speed ω_{ref} and the actual motor speed ω_m

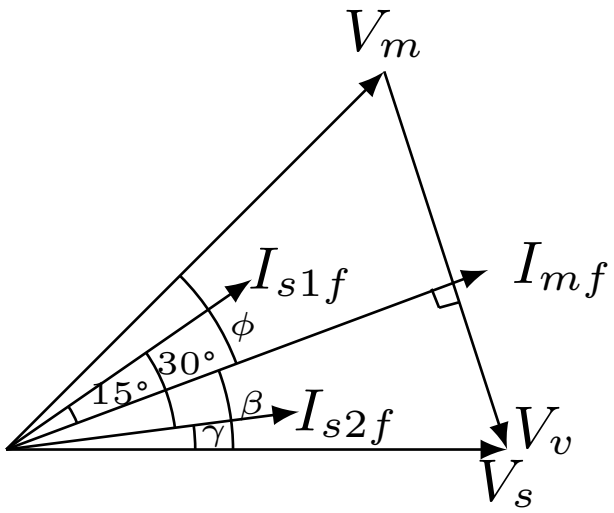

Figure 3.8: Phasor diagram showing CSI terminal voltage (V_s), motor voltage (V_m), VSI output voltage (V_v) and fundamental components of motor current (I_{mf}), CSI-1 current (I_{s1f}), CSI-2 current (I_{s2f}).

is processed by a speed controller to obtain the slip speed ω_{slip}. Tight control on the slip speed is established by the slip limit block. The DC-link current is controlled to meet the load torque demand. The reference for DC-link current is generated by the current reference block which is a look-up table based on the ω_{slip} and the RMS value of the fundamental component of the motor current 'i_{mrms}'. The relationship between 'i_{mrms}' and the DC-link current '$\frac{i_{dref}}{2}$' can be obtained from the Fourier series expansion of the actual motor current. In Equation 3.9, by substituting δ=30° the Fourier coefficient corresponding to the fundamental component(b_1) can be obtained as :

$$b_1 = \frac{4}{\pi} \cdot 1.67 \cdot i_d \tag{3.17}$$

So, the fundamental component of motor current i_{mf} can be written as:

$$i_{mf} = b_1 sin(\omega t) \tag{3.18}$$

By substituting eq.(3.17) in eq.(3.18), the motor current fundamental i_{mf} as a function of DC-link current i_d can be written as,

$$i_{mf} = \frac{4}{\pi} \cdot 1.67 \cdot i_d \cdot sin(\omega t) \tag{3.19}$$

Hence, the RMS value of the fundamental component of the motor current fundamental would be:

$$i_{mrms} = \frac{4}{\sqrt{2}\pi} \cdot 1.67 \cdot i_d \tag{3.20}$$

The DC-link current to be maintained by the individual current controllers '$\frac{i_{dref}}{2}$' as a function of the RMS current of motor (i_{mrms}) is obtained as below,

$$\frac{i_{dref}}{2} = \frac{\sqrt{2}\pi}{8 \times 1.67} \cdot i_{mrms} \tag{3.21}$$

The DC-link current reference '$\frac{i_{dref}}{2}$' obtained from Equation (3.21), is maintained by the current controllers (current controller-1 and current controller-2) of Rectifier-1 and Rectifier-2. This is done by varying the firing angles 'α_1' and 'α_2' of Rectifier-1 and Rectifier-2 respectively. The firing angles are obtained by dividing the outputs of the current controllers V_{rec-1} and V_{rec-2} with the rectifier gain (G_{rec}), as discussed in Chapter-2 of the thesis. The firing angles α_1 and α_2 are used to generate the triggering pulses of the SCRs of Rectifier-1 (G_{Tru1} to G_{Tru6}) and Rectifier-2 (G_{Trl1} to G_{Trl6}) respectively. The synchronous frequency ω_s to be maintained by the multilevel CSI (both CSI-1 and CSI-2) is obtained by adding the slip speed (ω_{slip}) and the actual motor speed (ω_m). Three phase sinusoidal signals of unit magnitude, with frequency ω_s are then generated for creating the gating pulses of the SCRs of CSI-1 and CSI-2. Since, the CSIs are operated with a phase shift of 30° the three-phase sinusoidal signals used for generating the firing pulses of CSI-1 (i_{ga1},i_{gb1},i_{gc1}) and CSI-2 (i_{ga2},i_{gb2},i_{gc2}) will also have a phase shift of 30° between them as shown in Figure 3.10. The three-phase sinusoidal signals used for generation of the firing pulses of CSI-1 (i_{ga1},i_{gb1},i_{gc1}) can be written as,

$$i_{ga1} = sin(\omega t) \tag{3.22}$$

$$i_{gb1} = sin(\omega t - 120°) \tag{3.23}$$

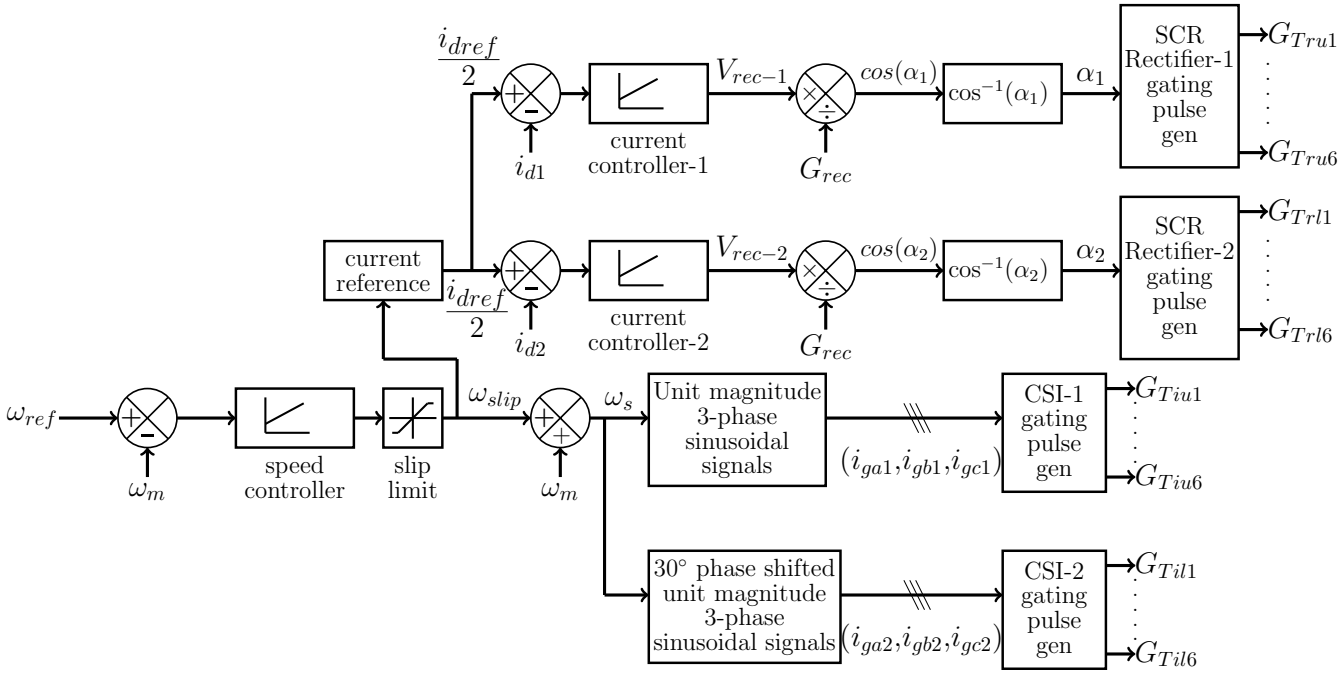

Figure 3.9: Control scheme of multilevel CSI.

$$i_{gc1} = sin(\omega t - 240°) \tag{3.24}$$

And the unit magnitude three phase sinusoidal of CSI-2 would be,

$$i_{ga2} = sin(\omega t - 30°) \tag{3.25}$$

$$i_{gb2} = sin((\omega t - 120°) - 30°) \tag{3.26}$$

$$i_{gc2} = sin((\omega t - 240°) - 30°) \tag{3.27}$$

These three phase sinusoidal signals are used for SCR gating pulse generation of CSI-1 (G_{Tiu1} to G_{Tiu6}) and CSI-2 (G_{Til1} to G_{Til6}), for their 120 degree mode of operation.

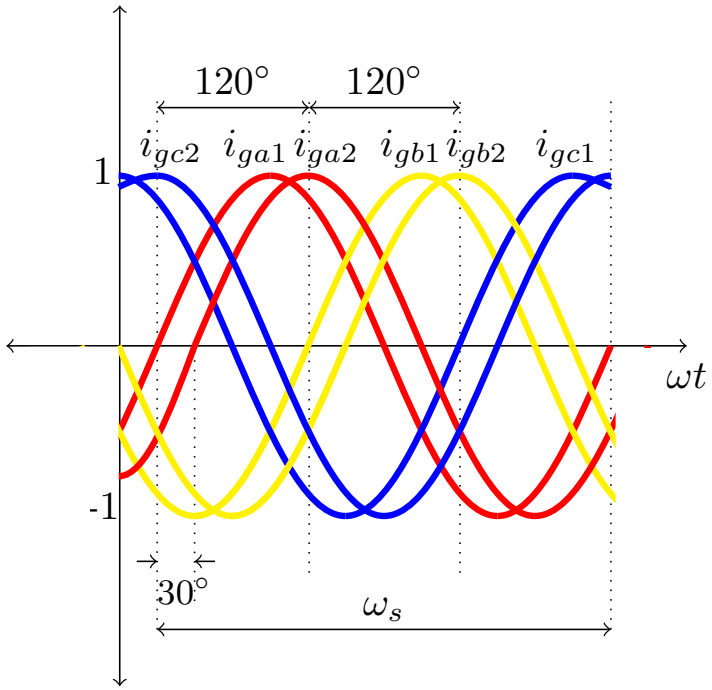

Figure 3.10: Unit magnitude three phase sinusoidal signals for SCR firing pulse generation of CSI-1 and CSI-2.

3.5.2 Control scheme of the VSI

The role of VSI is to facilitate load commutation of CSIs, by keeping the fundamental component of the motor current leading ahead of the CSI terminal voltage under all conditions of motor operation. This necessitates both the VSI and the CSI to be operated in synchronism. The control scheme of the VSI is implemented on a synchronously rotating (d-q) reference frame oriented along the motor current phasor as depicted in Figure 3.12. The fundamental components of three phase motor currents (i_{maf}, i_{mbf} and i_{mcf}) determined using the gating signal information of CSI-1 (i_{ga1},i_{gb1},i_{gc1}) and the DC-link current (i_d), can be used for unit vector generation required for the d-q (synchronous frame) transformation. Since, the phasor (I_{mf}) representing the fundamental component of the motor current lags behind the phasor representing the fundamental component of the CSI-1 current (I_{s1f}) by 15° as shown in Figure 3.8, by using Equation 3.19 the fundamental component of A-phase motor current (i_{maf}) can be written as:

$$i_{maf} = \frac{4}{\pi} \cdot 1.67 \cdot i_d \cdot sin(\omega t - 15°) \tag{3.28}$$

Similarly, the fundamental component of motor currents in B-phase (i_{mbf}) and C-phase (i_{mcf}) can be written as given in Equation 3.29 and 3.30 respectively.

$$i_{mbf} = \frac{4}{\pi} \cdot 1.67 \cdot i_d \cdot sin((\omega t - 120°) - 15°) \tag{3.29}$$

$$i_{mcf} = \frac{4}{\pi} \cdot 1.67 \cdot i_d \cdot sin((\omega t - 240°) - 15°) \tag{3.30}$$

The fundamental components of the three phase motor currents (i_{maf},i_{mbf},i_{mcf}) are first transformed from abc reference frame to $\alpha - \beta$ (stationary) reference frame to obtain their components along α-axis ($i_{mf\alpha}$) and β-axis ($i_{mf\beta}$), which are used to generate unit vectors for transformation to rotating reference frame. Also, the terminal voltages of the CSI (v_{sa}, v_{sb} and v_{sc}) derived from the sensed multilevel CSI line voltages are first transformed to $\alpha - \beta$ frame, and then to the rotating d-q reference frame using the unit vectors derived from $i_{mf\alpha}$ and $i_{mf\beta}$ to obtain the d-axis (V_{sd}) and q-axis (V_{sq}) components. The filtered values V_{sdf} and V_{sqf} (corresponding to the fundamental components) of V_{sd} and V_{sq} respectively are extracted using a low pass filter (LPF) with cut-off frequency of 1Hz. Figure 3.11 shows the system phasor diagram in d-q reference frame, where the phasor 'I_{mf}' representing the fundamental component of motor current leads ahead of the phasor 'V_s' representing the CSI terminal voltage by an angle 'β'. The d-axis and q-axis components of 'V_s' ie. V_{sdf} and V_{sqf} respectively are marked in Figure 3.11. If the ratio between V_{sdf} and V_{sqf} as given in Equation 3.31 can be maintained, then lead angle 'β' can be ensured at the CSI terminal.

$$tan(\beta) = \frac{V_{sqf}}{V_{sdf}} \tag{3.31}$$

This lead angle (β) is ensured by the q-axis controller of the VSI by generating sufficient q-axis component of the VSI voltage (V_{vq}). The complete control scheme of VSI including all the transformations is depicted in Figure 3.12. In Figure 3.11 the d-axis

component of the VSI voltage(V_{vd}) is neglected as its value is very small compared to that of V_{vq}, since the VSI draws only a very small amount of active power to meet the losses in the inverter and the capacitor. The q-axis controller reference(V_{sqref}) for reactive power control, in order to maintain the lead angle β can be obtained from Equation 3.32.

$$V_{sqref} = -tan(\beta) * V_{sdf} \tag{3.32}$$

Since the VSI is controlled to supply only the reactive power to the system, a pre-charged capacitor is sufficient to hold its DC-link voltage. The VSI can supply the required reactive power only if its capacitor (C) voltage is maintained at the required minimum level. The power losses in the inverter and capacitor will result in reduction in the capacitor voltage. Hence, a closed loop control is required for balancing of the capacitor voltage. The d-axis PI controller shown in Figure 3.12 is employed for this purpose. It generates sufficient 'V_{vd}' value to ensure that adequate active power is drawn by the VSI to meet the losses in the inverter and capacitor, so that the capacitor voltage (V_c) is maintained at the reference value (V_{cref}). The outputs of the controllers along d-axis and q-axis (V_{vd} and V_{vq} respectively) are then transformed to the stationary ($\alpha - \beta$) reference frame to obtain $v_{v\alpha}$ and $v_{v\beta}$. The three phase modulating signals v_{vam}, v_{vbm} and v_{vcm} for the VSI are then obtained by transformation from ($\alpha - \beta$) to the three-phase (abc) reference frame for generation of gating pulse for the IGBTs.

3.6 Regenerative Braking

One of the key features of the CSI fed drive is its inherent capability for regenerative braking without requirement of any additional circuit. Regeneration control is activated when the machine speed reference is stepped down to a lower value and also during speed reversal. Under these conditions the induction machine acts as generator feeding back the energy stored in the inertia of the motor and the load to the AC supply. Figure 3.13 shows the waveforms of the CSI terminal voltage (v_{sa}) and the machine current (i_{ma}) in

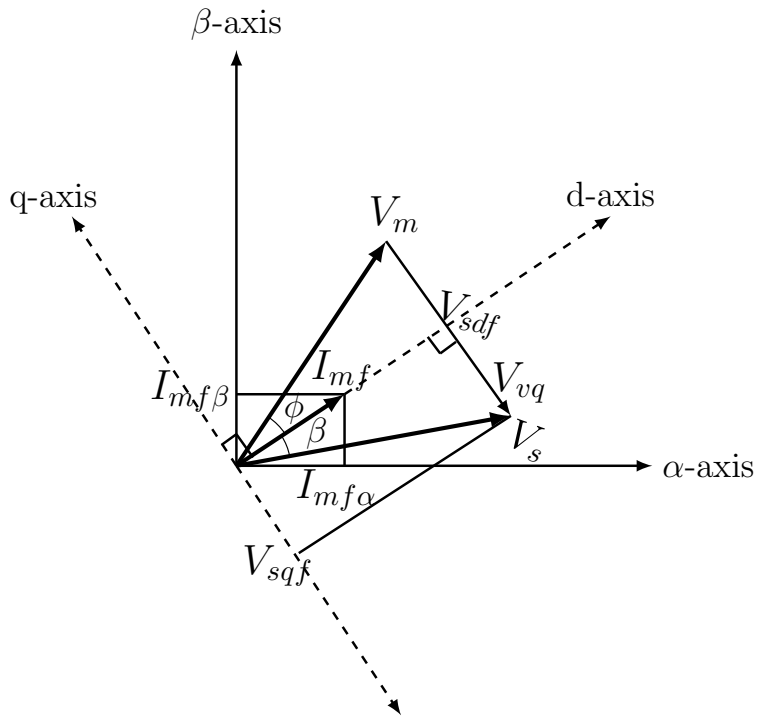

Figure 3.11: Phasor diagram showing the orientation of d-q axes, fundamental component of motor current (I_{mf}) and CSI terminal voltage (V_s).

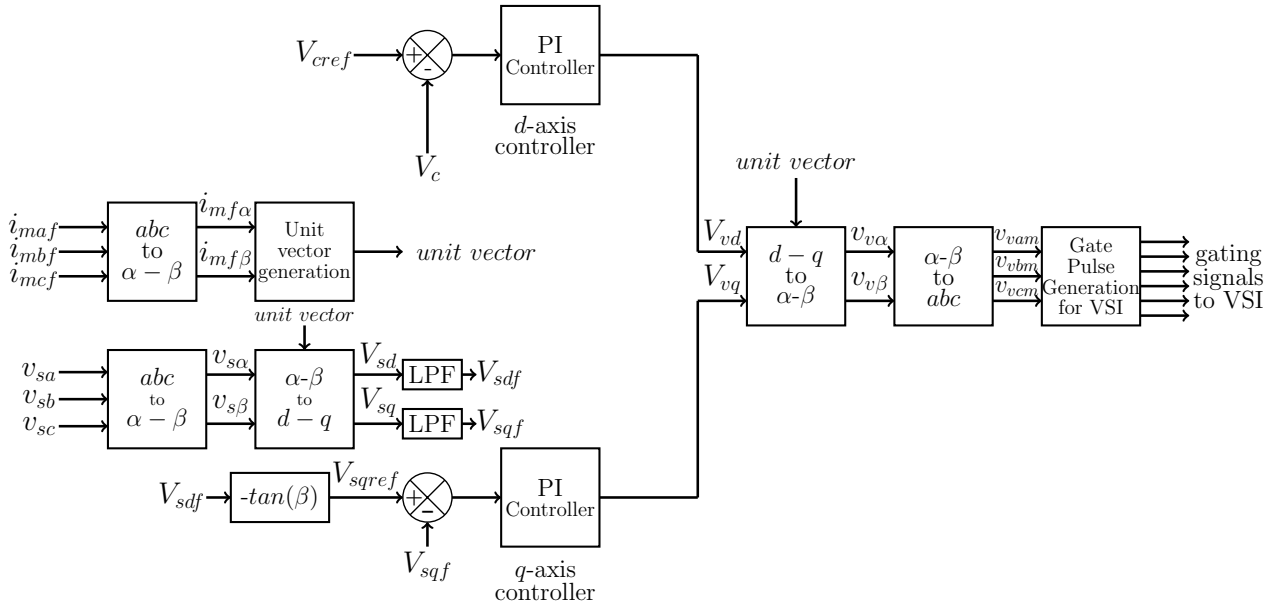

Figure 3.12: Control scheme of VSI.

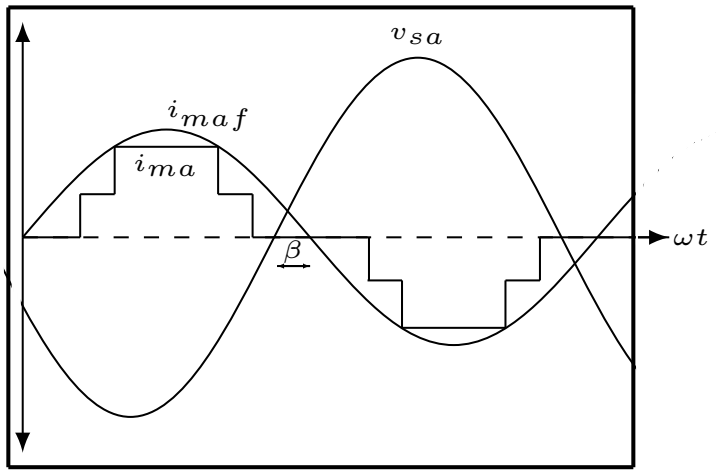

Figure 3.13: CSI terminal voltage (v_{sa}), machine current (i_{ma}) and its fundamental component (i_{maf}) during regeneration.

A-phase during regeneration. Figure 3.14 shows the phasor diagram depicting the machine voltage, the machine current, the CSI terminal voltage and the VSI output voltage during regeneration. The phase angle between the machine voltage V_m and the fundamental component of the machine current I_{mf} during regeneration is $(\pi - \phi)$, where ϕ is the power factor angle. During the regeneration the fundamental component of the motor current (I_{mf}) leads ahead of the CSI terminal voltage (V_s) by an angle $(\pi - \beta)$, where β is the phase angle between V_s and I_{mf} during the normal motor operation. The angle $(\pi - \beta)$ has to be maintained by the VSI during the regeneration for safe commutation. Since the filtered component of V_s along the d-axis (V_{sdf}) would be negative during the regeneration, the V_{sqref} is generated as given in Equation 3.33.

$$V_{sqref} = tan(\beta) * V_{sdf} \tag{3.33}$$

Pre-charging of the VSI capacitor:

The pre-charging of the VSI capacitor can be performed without any additional hardware. This is accomplished by triggering the top SCR of one phase and the bottom SCRs of another phase of CSI-1 and CSI-2 without providing the gating signals to the IGBTs of the VSI. A controlled DC current flows through the SCRs, motor windings and the anti-

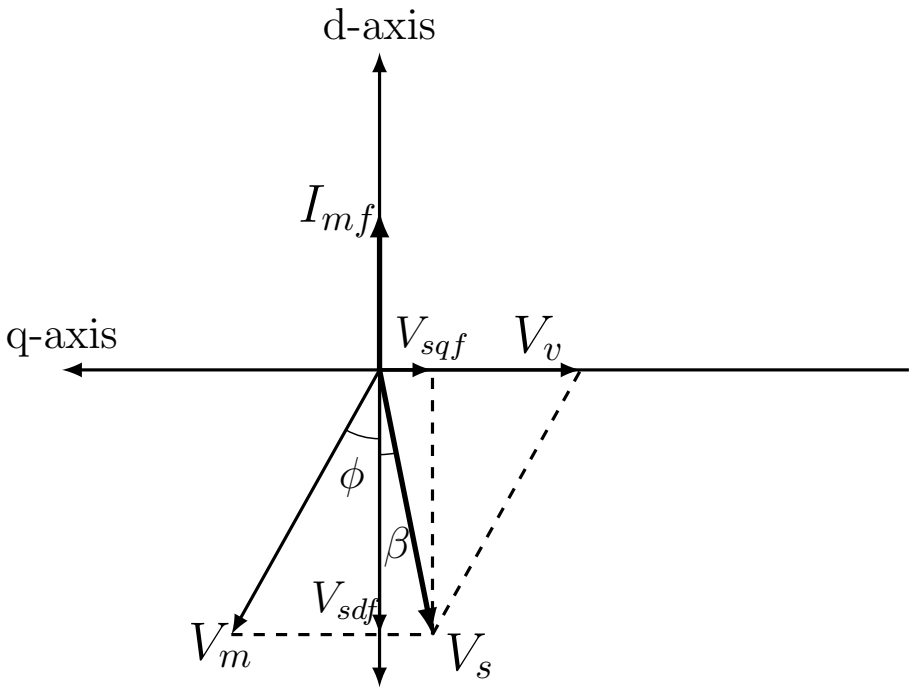

Figure 3.14: Phasor diagram during regeneration.

parallel diodes of the IGBTs to pre-charge the capacitor. Normal operation of the drive starts when the capacitor voltage reaches its reference value (V_{cref}). Figure 3.15 shows the pre-charging process where the SCRs of A-phase and B-phase of the multilevel CSI are triggered. The path of pre-charging current is marked red in colour.

3.7 Experimental results

The proposed scheme is experimentally verified on a 1.5 HP, 415 V, 50 Hz three phase induction motor with open-end stator windings. Rectifiers and current source inverters are built using converter grade SCRs of 1200V and 27A rating. Two identical DC link inductors of 200 mH are used to smoothen the output currents of the rectifiers; i_{d1} and i_{d2}. Hall effect based voltage and current sensors are used to sense the DC-link currents, the CSI terminal voltages and the VSI capacitor voltage. The VSI is built using IGBTs of 1200V and 75A rating with a voltage holding electrolytic capacitor of 2200 μF. The VSI is operated at a switching frequency of 1 kHz. Photograph of the experimental set-up is shown in Figure 3.16. The steady state and the transient performance of the drive are experimentally verified under different conditions. In addition, the low speed operation

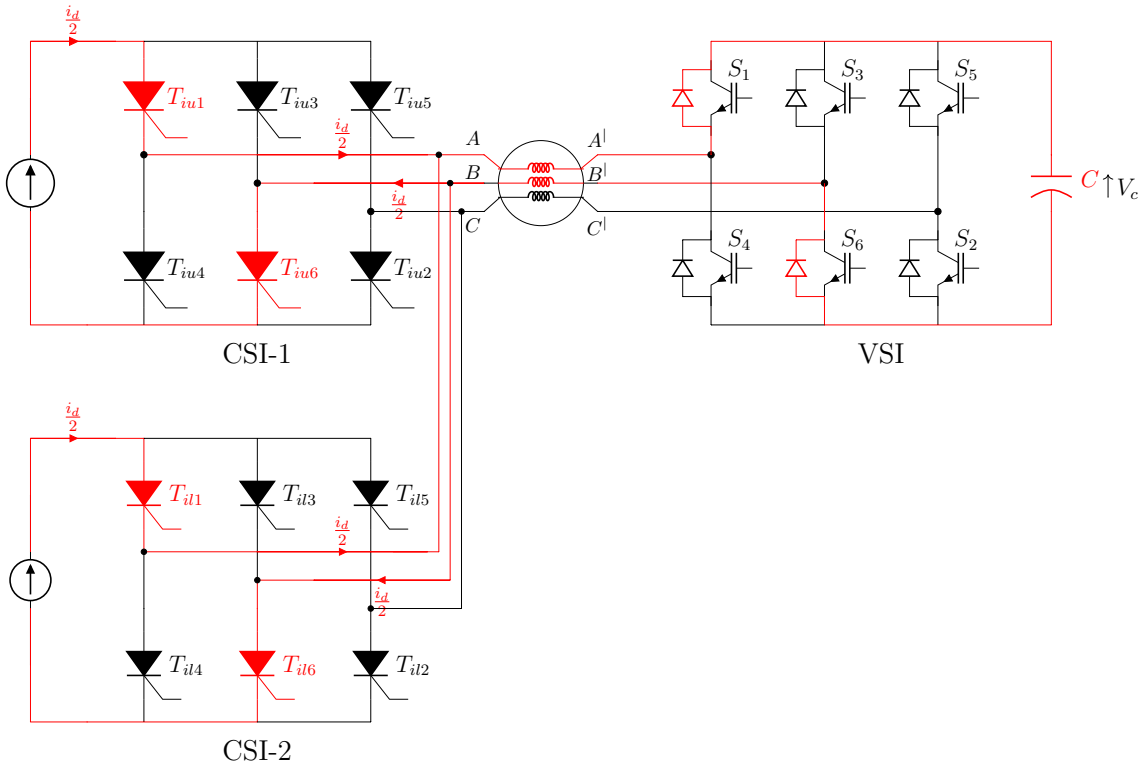

Figure 3.15: Pre-charging scheme for the capacitor of VSI.

of the drive and the capability to carryout regenerative braking are also verified. The experimental results are given in the following sections.

3.7.1 Steady state performance of the drive

Figure 3.17 shows the waveforms of the stator voltage of the motor measured across the open-end stator winding terminals, motor current, CSI-1 current and CSI-2 current in phase-A during 750 RPM operation. Figure 3.18 shows the actual DC link currents i_{d1}, i_{d2} and the DC-link current reference generated by the current reference block of the multilevel CSI control scheme. The gate triggering pulses of the top SCRs of the CSI-1 A-phase and CSI-2 A-phase are shown along with the motor A-phase stator voltage and current during 300 RPM (or 10 Hz) operation in Figure 3.19. The outputs (pulse train) of the pulse transformers used triggering the SCRs indicate the operation of the two CSIs phase shifted by 30 degrees. Figure 3.20 shows the waveforms when the motor is loaded. The A-phase motor current and the A-phase modulating voltage (v_{vam}) of the VSI are shown in Figure 3.21. Modulating voltage of the VSI is captured using uni-polar digital

Figure 3.16: Photograph of the experimental setup

to analog converter (DAC) of the DSP, and then level-shifted by a unit division so as to observe the bipolar modulating signal. It can be observed that the phase difference between the VSI modulating voltage and the motor current is close to 90 degrees which substantiates that only reactive power is provided by the VSI.

3.7.2 Transient performance of the drive

Figure 3.22 shows the stator voltage of motor in A-phase and the VSI capacitor voltage when the motor is accelerated from 300 to 1000 RPM. It can be seen that the VSI capacitor voltage is constant throughout the period of acceleration, proving the effectiveness of the capacitor voltage balancing scheme. Motor response for a step change in speed reference is shown in Figure 3.23.

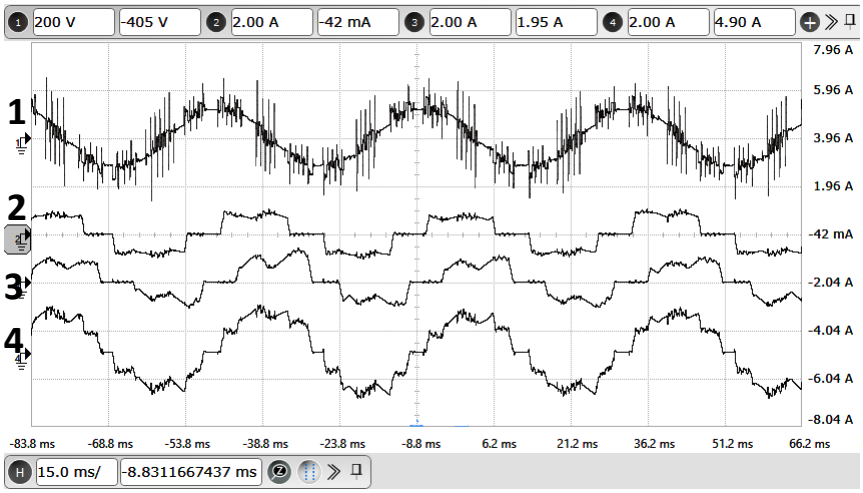

Figure 3.17: Experimental results : Motoring operation at 750 RPM: X-axis: 15ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 200 V/div). Ch-2: A-phase CSI-1 current (Y-axis: 2 A/div). Ch-3: A-phase CSI-2 current (Y-axis: 2 A/div). Ch-4: A-phase motor current (Y-axis: 2 A/div).

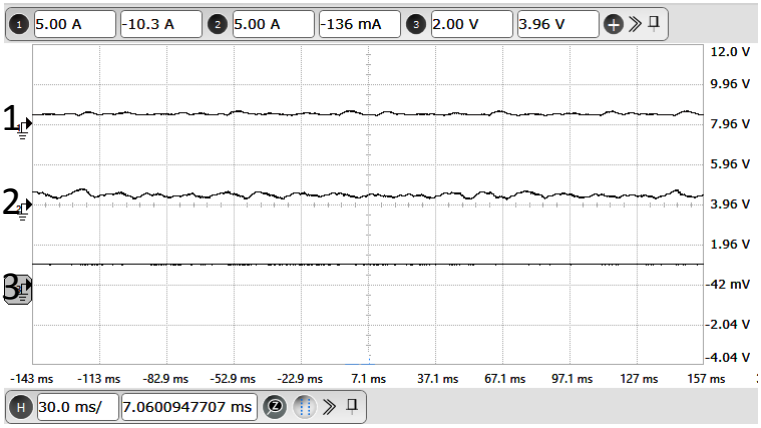

Figure 3.18: Experimental results : Ch-1: Actual DC-link current i_{d1} (Y-axis: 5 A/div). Ch-2: Actual DC-link current i_{d2} (Y-axis: 5 A/div). Ch-3: DC-link current reference captured using digital to analog Converter (DAC) of DSP (Y-axis: 2 A/div).

3.7.3 Low speed operations of the drive

One of the major drawbacks of the conventional load commutated CSI-fed drive is the commutation failure during low speed operation, due to insufficient motor back EMF. While most of the CSI-VSI hybrid systems cited in this thesis need a separate scheme to run the drive at startup and low speeds, the proposed system is free from such deficiency since the VSI can provide enough voltage as well as lead angle for natural commutation of the SCRs. In the proposed system the induction motor can be operated at low speeds with

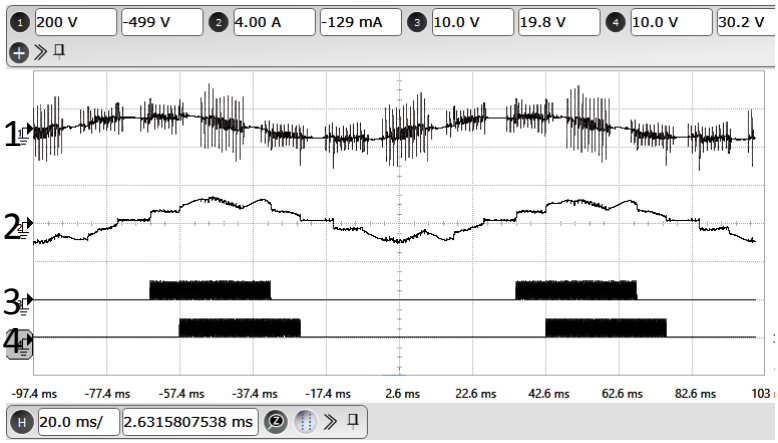

Figure 3.19: Experimental results : 300 RPM (or 10 Hz) motor operation: X-axis: 20 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 200 V/div). Ch-2: A-phase motor current (Y-axis: 4 A/div). Ch-3: CSI-1 A-phase top SCR triggering pulse (Y-axis: 10 V/div). Ch-4: CSI-2 A-phase top SCR triggering pulse (Y-axis: 10 V/div).

full load torque without the problem of commutation failure. Figure 3.24 shows motor operation at 100 RPM.

3.7.4 Harmonic analysis of the motor current

The multilevel CSI configuration is primarily proposed for reducing the harmonic content of the motor current. Harmonic analyses of the quasi-square wave current of the two-level CSI and the multilevel motor current of the proposed system is presented in this section. For quasi square wave motor current, instead of operating both CSI-1 and CSI-2, only CSI-1 is operated at a leading power factor. Figure 3.25 shows the stator voltage and current in A-phase winding of the motor for single CSI operation. Harmonic analysis of the quasi square wave motor current is shown in Figure 3.26. 5^{th} and 7^{th} harmonic contents are approximately 20% and 13% respectively, during the single CSI operation. Figure 3.28 shows the harmonic contents of the motor current shown in Figure 3.27 for multilevel CSI operation. A significant reduction in the 5^{th} and 7^{th} contents can be observed because of the 30 degrees phase shifted operation of the CSI-1 and the CSI-2. As presented in [77] the reduction in 5^{th} and 7^{th} harmonic currents will bring down the 6^{th} harmonic torque pulsations in the motor substantially.

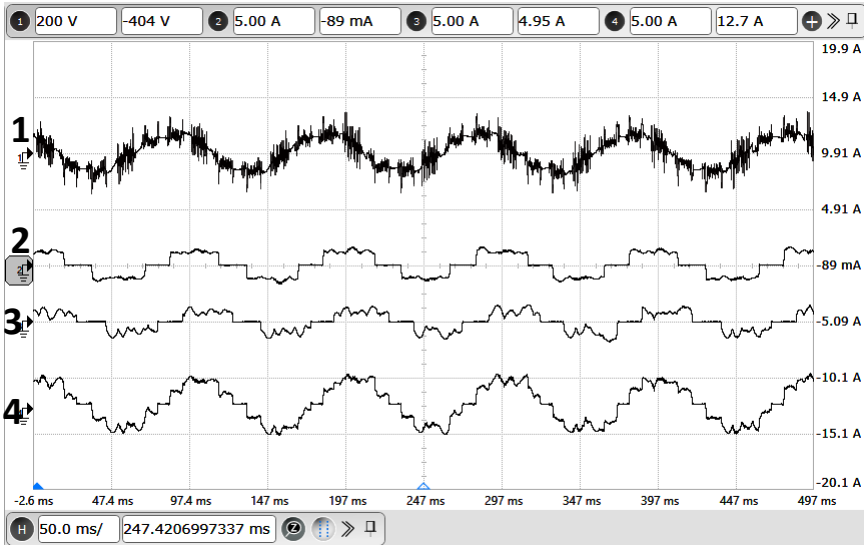

Figure 3.20: Experimental results: Motoring operation at 300 RPM with load: X-axis: 50 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 200 V/div). Ch-2: A-phase CSI-1 current (Y-axis: 5 A/div). Ch-3: A-phase CSI-2 current (Y-axis: 5 A/div). Ch-4: A-phase motor current (Y-axis: 5 A/div).

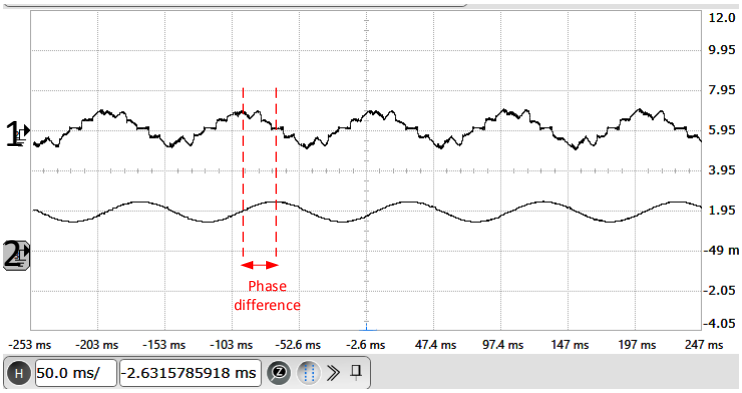

Figure 3.21: Experimental results: X-axis: 50 ms/div. Ch-1: A-phase motor current (Y-axis: 5 A/div). Ch-2: A-phase modulating voltage of VSI captured using unipolar DAC of DSP, the bipolar modulating signal is DC shifted by a unit division (Y-axis: 0.5 unit/div) .

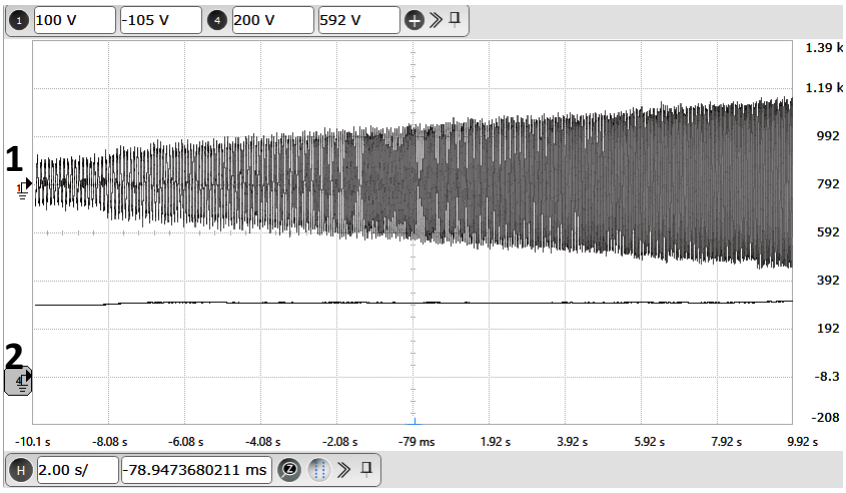

Figure 3.22: Experimental results : Acceleration of motor from 300 to 1000 RPM: X-axis: 2 s/div. Ch-1: A-phase stator voltage of motor (Y-axis: 100 V/div). Ch-2: VSI capacitor voltage V_c (Y-axis: 200 V/div).

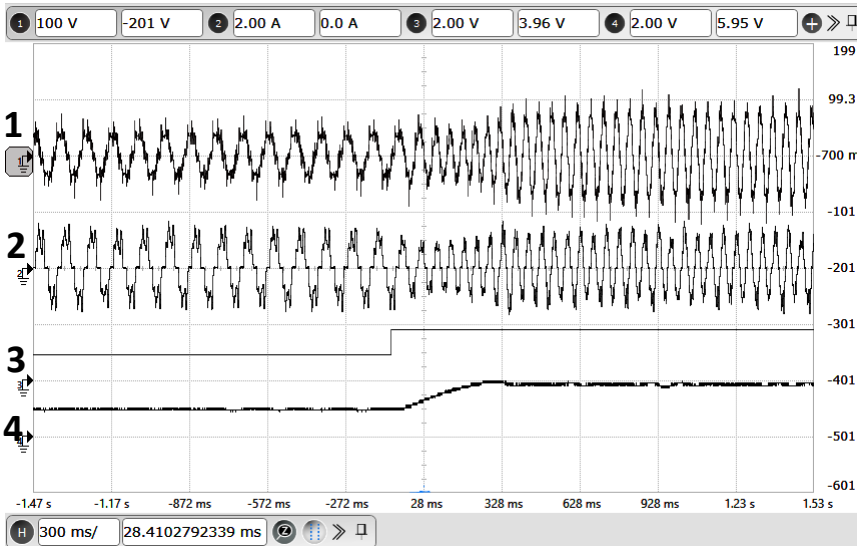

Figure 3.23: Experimental results: Step change in motor speed from 300 RPM to 600 RPM: X-axis: 300 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 2 A/div). Ch-3: Motor speed reference (Y-axis: 666 rpm/div). Ch-4: Actual motor speed (Y-axis: 666 rpm/div).

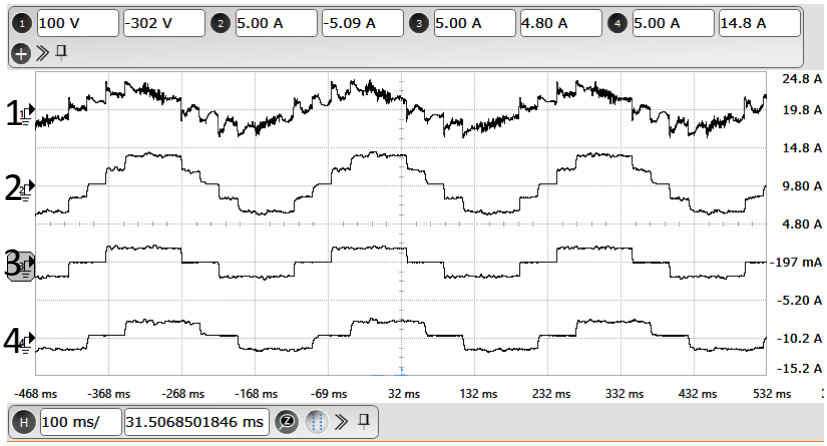

Figure 3.24: Experimental results during low speed operation at nearly rated torque (100 RPM): X-axis: 100 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div). Ch-3: A-phase CSI-1 current (Y-axis: 5 A/div). Ch-4: A-phase CSI-2 current (Y-axis: 5 A/div).

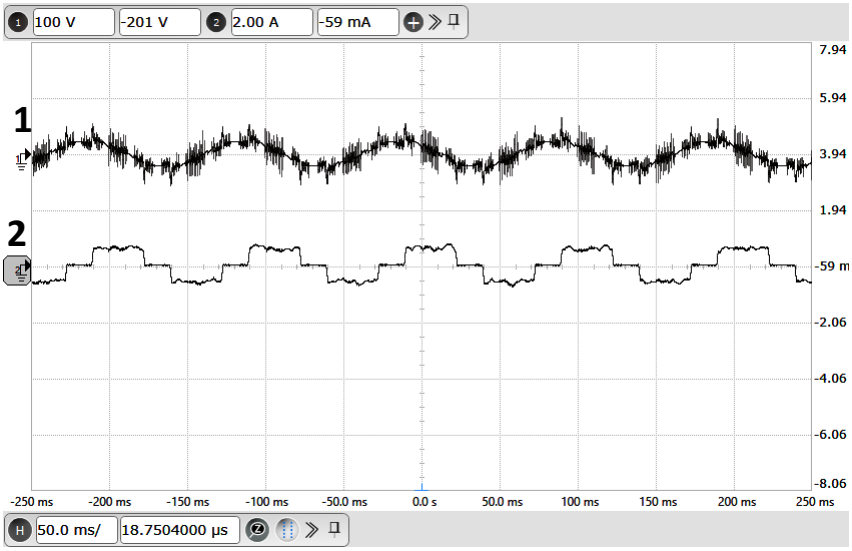

Figure 3.25: Experimental results: Motor operation at 300 RPM with single CSI: X-axis: 50 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 2 A/div).

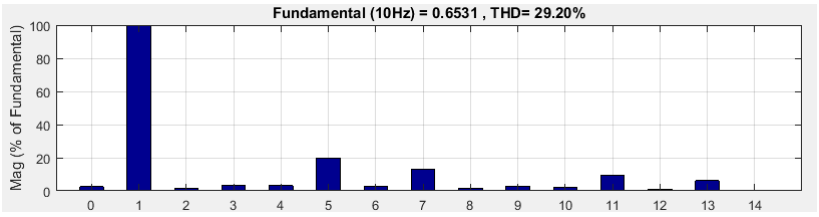

Figure 3.26: Harmonic spectrum of motor current shown in Fig.3.25 with single CSI operation: X-axis (Harmonic order). Y-axis: (Magnitude in % of fundamental).

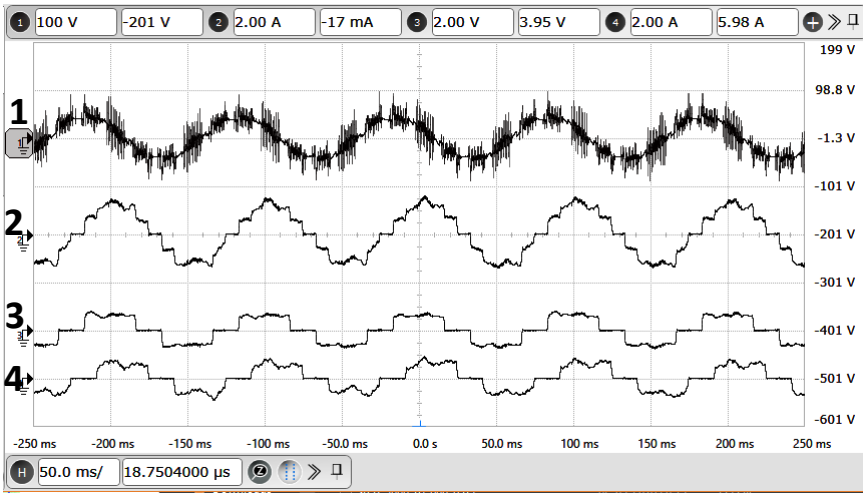

Figure 3.27: Experimental results: Motor operation at 300 RPM with multilevel CSI: X-axis: 50 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 2 A/div). Ch-3: A-phase CSI-1 current (Y-axis: 2 A/div). Ch-4: A-phase CSI-2 current (Y-axis: 2 A/div).

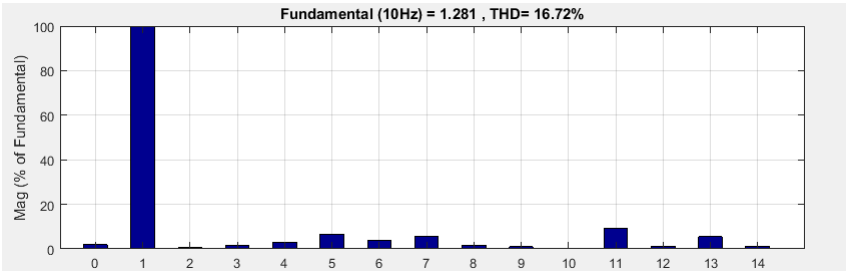

Figure 3.28: Harmonic spectrum of the motor current with multilevel CSI operation : X-axis (Harmonic order). Y-axis: (Magnitude in % of fundamental).

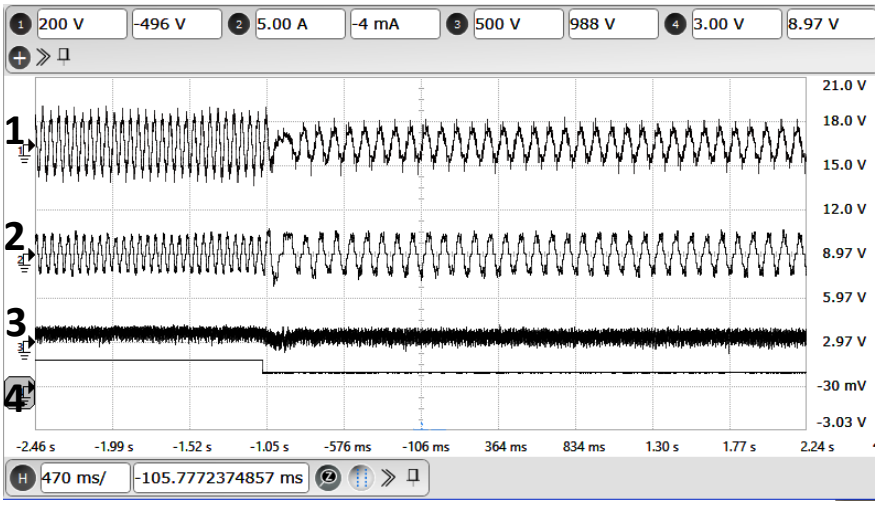

Figure 3.29: Experimental results: Regenerative braking of the drive during step change in motor speed from 600 RPM to 300 RPM : X-axis: 470 ms/div. Ch-1: A-phase stator voltage of motor (Y-axis: 200 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div). Ch-3: DC link voltage of Rectifier-1 (Y-axis: 500 V/div). Ch-4: Motor speed reference (Y-axis: 333 rev/min/div).

3.7.5 Experimental verification of the regenerative braking of the drive

Figure 3.29 shows the experimental result during regenerative braking operation of the drive when a step change in motor speed is commanded from 600 RPM to 300 RPM. Trace-3 of this result shows the DC-link voltage of Rectifier-1. It can be observed that the DC-link voltage becomes negative during the period of regeneration identically in both Rectifier-1 and Rectifier-2 indicating the reverse power flow from DC sides of the rectifiers to the AC source.

3.8 Conclusion

A new configuration of the load commutated SCR based multilevel current source inverter (CSI) fed open-end winding induction motor drive is presented in this chapter. This configuration consists of two SCR based current source inverters connected to one side of the stator windings and a capacitor-fed voltage source inverter connected to the other side. The current source inverters are operated in a phase shifted manner to realize multi-

level current waveform in the motor. The current source inverters provide the real power requirement of the system. The VSI is used for supplying adequate reactive power to operate the multilevel CSI at leading power factor so as to ensure load commutation under all conditions, including regeneration. The multilevel waveform significantly improves the quality of the motor current. Harmonic analysis of the motor current shows significant reduction in the 5^{th} and 7^{th} harmonic contents compared to that of a two-level CSI fed IM drive. The substantial reduction in the lower order harmonics results in significant reduction in the torque pulsations and the losses due to harmonics. Another attractive feature of the proposed drive scheme is its capability to operate at low speeds, providing full load torque, without any problems like commutation failure normally encountered in load commutated CSI fed drives at low speeds due to insufficient back EMF. The performance of the proposed drive system is experimentally verified under all conditions of operation including regenerative braking. The concept of using VSI as a series compensator of reactive power can be extended to the traditional load commutated synchronous motor drive to address the issue of commutation failure during low speed operation due to insufficient back-EMF. This topic is presented in the next chapter.

Chapter 4

A Series Voltage Compensated Synchronous Motor Drive with Load Commutation during Starting and Low Speed Operation

4.1 Introduction

A major problem faced in the conventional load commutated current source inverter (CSI) fed synchronous motor drive is the commutation failure during low speed operation due to insufficient back-EMF to turn OFF the SCRs [47]. For the same reason it will not be possible to achieve load commutation during the startup of the motor since the back-EMF will be zero initially. Hence forced commutation based systems have been suggested for its starting and low speed operation as presented in [78, 79, 80, 77]. Another scheme adopted in the industry for starting and low speed operation of CSI fed synchronous motor drive is known as pulsed mode operation or DC-link current pulsing [48, 81]. In the pulsed mode of operation, in order to turn OFF SCR the DC-link current is reduced to zero by controlling the rectifier. During the period of commutation of one SCR since the DC-link current becomes zero, all other SCRs of the CSI also get turned OFF. The DC-link current is then re-established to its normal value and the switching of the CSI is resumed. Pulsed mode of operation is continued till the motor reaches sufficient speed, so that the motor back-EMF can facilitate commutation. In practice, this pulsed mode of operation is continued till the motor attains 10 % of its rated speed, known as the change over speed [82]. The current pulsing results in high motor torque pulsations at the pulsing frequency [77, 83]. These torque pulsations at low frequency can excite mechanical resonance of the drive train in high power drive applications, which may even result in motor shaft failures. The transition time of the drive from the current pulsing mode to the normal commutation mode is considerable, making the starting process very lengthy. The loss

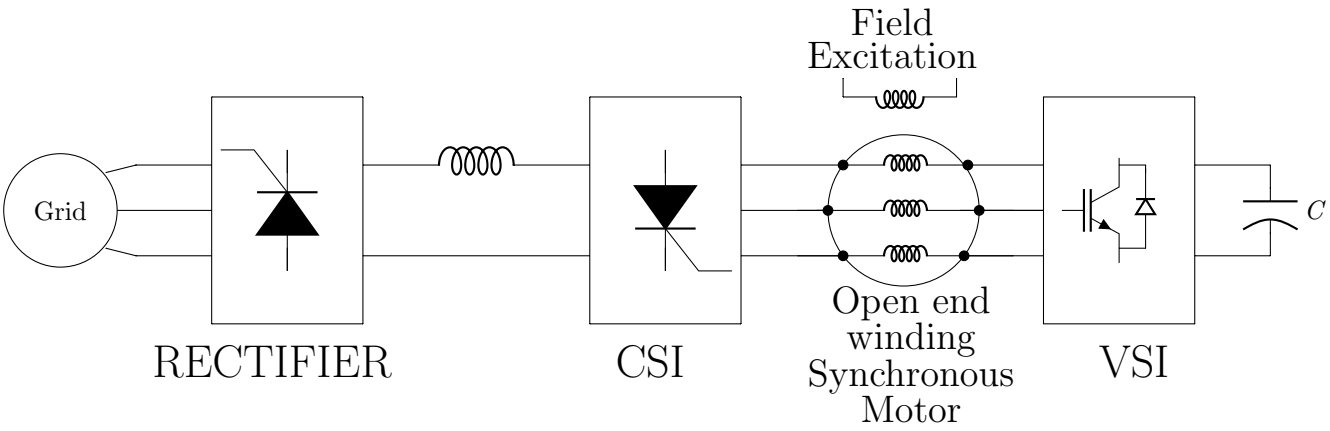

Figure 4.1: Block diagram of the proposed load commutated open-end winding synchronous motor drive.

of current time area during pulsed mode reduces the capability of the drive to deliver high starting torque. A hybrid system consisting of a load commutated CSI and a VSI connected at the motor terminal, which obviates the need for current pulsing during low speed operation, is presented in [84]. In this scheme the motor is started and run using the VSI till the motor reaches the changeover speed. Thereafter the operation of the load commutated CSI starts and the VSI is operated as a shunt harmonic filter resulting in an almost sinusoidal motor current. However, this system requires an additional rectifier and an interfacing inductor, thereby increasing the hardware complexity. Also, since the VSI is rated for harmonic compensation alone, the drive cannot deliver high load torque during start-up and low speed operation.

This chapter presents a hybrid system consisting of a CSI and a VSI for synchronous motor drive with open-end stator windings to achieve load commutation in the entire range of speed, without resorting to pulsed mode operation even at the time of starting. Figure 4.1 shows the block diagram of the proposed scheme which consists of a SCR based CSI connected to one side of the open-end stator windings of the synchronous motor; while the other side of the windings is connected to a capacitor-fed IGBT based voltage source inverter (VSI). The CSI provides the real power requirement of the system, while the VSI is controlled to generate sufficient voltage which gets added vectorially to the motor back-EMF to facilitate load commutation during the start-up and the low speed operation. When the drive speed exceeds the changeover speed the operation of the VSI can be stopped since there will be sufficient back-EMF in the motor to facilitate commutation of

the SCRs. Then the VSI-side ends of the stator windings can be shorted either by using electro-mechanical contactors or by turning ON all the upper (or lower) switches of the VSI. Alternatively, the VSI operation can be continued in the entire speed range thereby facilitating easy four quadrant operation.

4.2 Power circuit of the proposed series voltage compensated synchronous motor drive

Figure 4.2 shows the power circuit diagram of the proposed topology. The current source consists of a line commutated SCR based rectifier with an inductor (L_{dc}) filter at its output. Through closed loop operation, the DC-link current (i_d) is maintained at its reference value. SCR based CSI connected to one side of the stator windings is operated in 120 degrees mode of conduction, resulting in a quasi-square wave motor current. The other side of the stator windings is connected to an IGBT based VSI having a voltage holding capacitor 'C'. The VSI is used to inject a voltage to the motor winding which gets vectorially added to the back-EMF so as to facilitate load commutation of the CSI, during the periods of starting and low speed operations. Once the motor reaches the changeover speed (usually around 10% of rated speed of motor) the VSI operation can be stopped and the system can be operated as a conventional over-excited synchronous motor drive with star connected windings. As already stated this can be done either by using electro-mechanical contactors or by turning ON the entire upper (or lower) switches of the VSI. Over-excitation of the synchronous motor ensures that the motor current is leading ahead of the CSI terminal voltage. In addition the back-EMF generated will be sufficient to ensure load commutation of the SCRs of the CSI. Figure 4.3 shows the phasor diagram of the system when VSI is in operation. The motor voltage (V_m) lags behind the fundamental component of motor current (I_{mf}) by angle 'γ' because of the over-excited operation of the synchronous motor. The VSI impresses a voltage (V_v) on the motor winding in quadrature with the motor current. The CSI terminal voltage (V_s) is the resultant of the voltage vectors V_m and V_v as given in Equation (4.1).

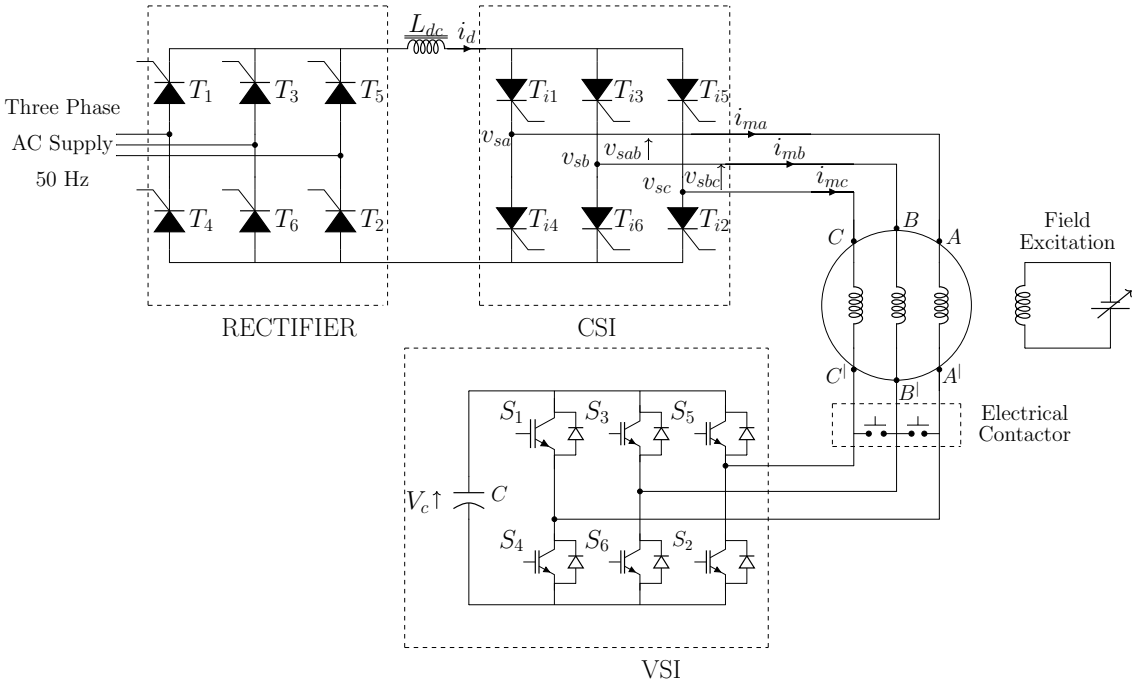

Figure 4.2: Complete Power Circuit diagram of the proposed scheme.

$$\vec{V_s} = \vec{V_m} + \vec{V_v} \tag{4.1}$$

The magnitude of the CSI terminal voltage (V_s) to be established using the VSI is determined based on the magnitude of the reverse voltage required to turn OFF the outgoing SCR of the CSI. The fundamental component of motor current (I_{mf}) leads ahead of the CSI terminal voltage (V_s) by an angle β, as shown in Figure 4.3. This lead angle β would also ensure that sufficient time is provided for the turn OFF of the SCRs. Since the VSI is required to supply only reactive power to the system it does not require a separate power source. Rather a voltage holding capacitor 'C' (Figure 4.1) is sufficient for its operation. A closed loop control scheme ensures that the voltage across the capacitor is maintained at the required level under all operating conditions. The capacitor voltage control scheme forces the VSI to draw a small amount of active power from the CSI only to meet the losses in the VSI and the capacitor. Hence the angle between the VSI voltage and the motor current will not be exactly 90 degrees.

When the motor attains sufficient speed (greater than 10% of rated speed) there is a choice of either keeping the VSI in operation or disconnecting it from the system. This

has to be decided based on the application. If the drive has to be operated only at high speed then the VSI operation can be stopped after the start-up and thereafter the machine can be operated as normal star connected over-excited synchronous motor. As stated in the previous section this can be done by either keeping all the upper (or lower) switches of the VSI in the ON state or using electrical contactors. However, if operation of the drive in low speed range or speed reversal without interruption is required then the VSI should be kept in operation even after the start-up. In this mode of operation the VSI will be used for achieving load commutation whenever the back-EMF is insufficient.

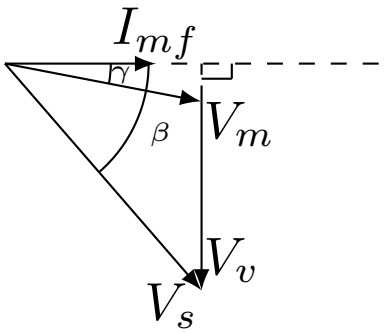

Figure 4.3: System phasor diagram with VSI in operation.

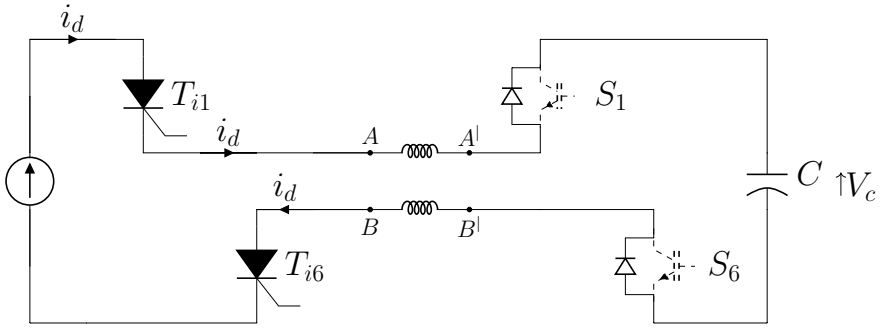

Figure 4.4: Pre-charging Scheme

4.3 Control Scheme

The primary aim of the control scheme is to facilitate load commutation of the CSI fed synchronous motor drive during start-up characterized by the absence of back-EMF and during low speed operation when the back-EMF is insufficient to commutate the SCRs of

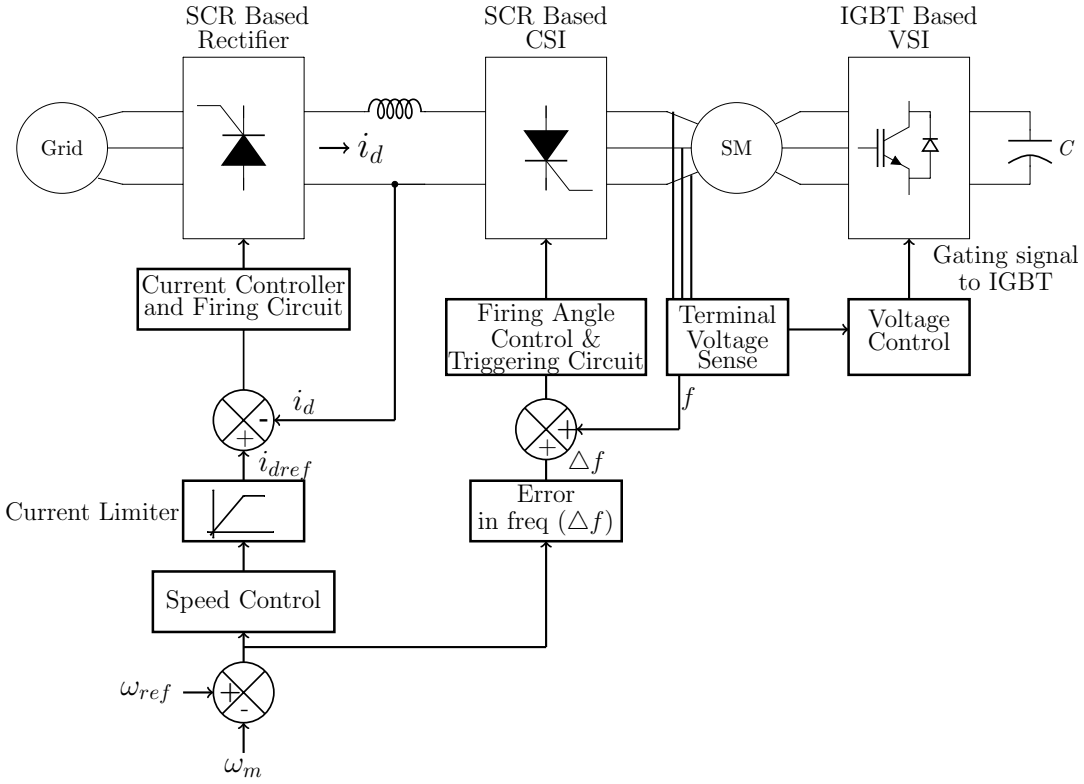

Figure 4.5: Synchronous motor speed control scheme.

the CSI. The VSI should be controlled to provide sufficient voltage to ensure load commutation under these conditions. However, to enable VSI operation its capacitor has to be pre-charged before the start-up since there is no power source connected to the DC link of the VSI. The proposed system does not require a separate circuit for the pre-charging of the VSI capacitor. Rather the CSI can be used for pre-charging the capacitor. To pre-charge the capacitor, the DC-link current (i_d) is allowed to flow through it by triggering upper SCR of one phase and lower SCR of another phase of the CSI. The capacitor charging current flows through the triggered SCRs, motor windings and anti-parallel diodes of the IGBTs of the corresponding phases of the VSI. During pre-charging gate pulses are not applied to the IGBTs of the VSI. The pre-charging process is depicted in Figure 4.4, with A-phase top SCR (T_{i1}) and B-phase bottom SCR (T_{i6}) in ON condition. Once the capacitor attains the required voltage (V_{cref}), the operation of the VSI starts. The drive control scheme involves variable frequency operation of the CSI by controlling the triggering of the SCRs and the control of the DC-link current by changing the triggering angle of the SCR based rectifier as per the load demand. Figure 4.5 shows the speed

control scheme of the proposed synchronous motor drive. The drive has an outer speed control loop and an inner current control loop. The actual speed of the motor (ω_m) is compared with the speed reference (ω_{ref}) and the error is processed by the speed controller to generate the current reference (i_{dref}) to attain the required speed and to meet the load torque demand. A current limiter is provided at the output of the speed controller. The current controller adjusts the triggering angle of the SCRs of the rectifier so as to match the actual DC-link current (i_d) with the DC-link current reference (i_{dref}). The switching frequency of the CSI is determined by adding the error in frequency ($\bigtriangleup f$) corresponding to the speed error, to the actual operating frequency (f) of the motor.

As already stated the role of the VSI is to maintain the required voltage at the CSI terminals to facilitate load commutation of the SCRs. In the conventional load commutated synchronous motor drive the back-EMF can support commutation, if the motor speed is more than 10% of its rated speed (called change-over speed). Hence, the approximate CSI terminal voltage (V_s) to be maintained using the VSI is 10% of the rated voltage of the motor (V_{mrated}). The control scheme of the VSI, implemented on a current oriented synchronously rotating reference (d-q) frame is shown in Figure 4.6. The q-axis controller of the VSI will be active only when the speed of the motor is less than 10% of the rated speed. When the speed exceeds the change-over speed the output of the q-axis controller of the VSI will be kept at zero value since voltage support from the VSI is not required for load commutation of SCRs at any speed greater than the change-over speed. When the speed is less than the change-over speed the CSI voltage (V_s) is compared with the reference voltage (V_{sref}) (aproximately 10% of the rated motor voltage) and the error is processed by a PI controller to generate the q-axis reference voltage of the VSI (V_{vq}).

The CSI line voltages v_{sab} and v_{sbc} (as in Figure(4.2)) are sensed to determine the CSI terminal voltages (or per phase voltages) v_{sa}, v_{sb} and v_{sc}. The CSI terminal voltages are first transformed to stationary two-axis ($\alpha - \beta$) reference frame using abc to ($\alpha - \beta$) transformation (Clarke transformation) to obtain $v_{s\alpha}$ and $v_{s\beta}$ respectively. The required magnitude of CSI terminal voltage (V_s) is maintained by monitoring the α and β components of V_s, namely $v_{s\alpha}$ and $v_{s\beta}$ respectively as in Equation 4.2.

$$V_s = \sqrt{v_{s\alpha}^2 + v_{s\beta}^2} \tag{4.2}$$

The q-axis controller ensures that sufficient q-axis component of VSI voltage (V_{vq}) is generated in order to keep the magnitude of CSI voltage (V_s) at the required value of 10% of the rated voltage of the motor. The reference value of the q-axis voltage is given by Equation 4.3.

$$V_{sref} = 0.1 * V_{mrated} \tag{4.3}$$

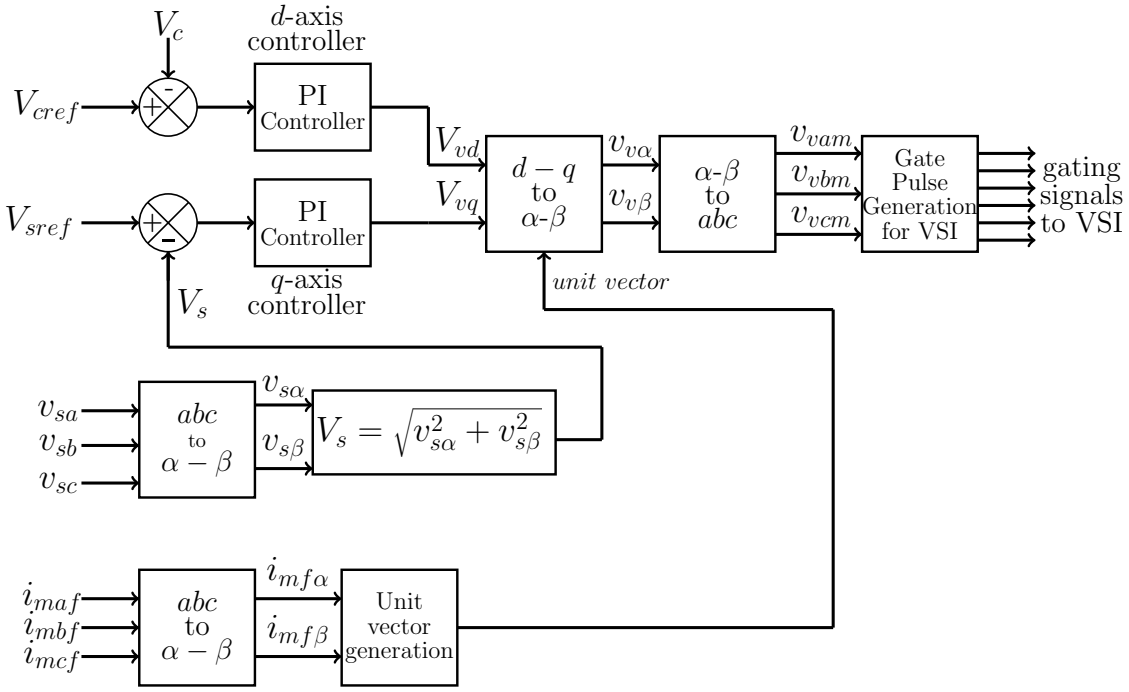

Figure 4.6: VSI control scheme.

Since the VSI is meant to supply only reactive power to the drive during its operation it can be fed by a pre-charged capacitor instead of a DC power source. But the capacitor voltage will drop from its pre-charged value during the operation of the drive due to the losses in the VSI and the capacitor. The function of the d-axis controller of the VSI is to maintain the capacitor voltage at the required level (V_{cref}) by drawing a small amount of active power from the CSI to compensate for the losses in the VSI and the capacitor. The d-axis controller output (V_{vd}) and the q-axis controller output (V_{vq}) of the VSI are then transformed to $\alpha - \beta$ reference frame and then to three-phase modulating

waveforms (v_{vam}, v_{vbm} and v_{vcm}) for switching of the VSI. Since the VSI has to operate in synchronism with the CSI, the reference waveforms for switching the VSI are obtained by transformation of the outputs of the d-axis and q-axis controllers to ($\alpha - \beta$) reference frame using the unit vectors derived from the fundamental components of the motor currents (CSI currents). The fundamental component of the motor currents in different phases (i_{maf}, i_{mbf}, i_{mcf}) can be derived from the gating signal information of the CSI and the DC-link current (i_d). Unit vectors can be obtained from the components of these currents in stationary ($\alpha - \beta$) reference frame ($i_{mf\alpha}$ and $i_{mf\beta}$). As already stated if the application demands frequent operation of the drive at low speed or speed reversal without interruption in the drive operation the VSI will continue to be in the system even after crossing the change over speed.

4.4 Experimental results

The proposed scheme is experimentally verified on a 3-HP open-end winding synchronous motor with ratings as 415 V, 3.4 A, 50 Hz, 1500 RPM. The current source is built using a SCR based controlled rectifier with a series inductor filter. Converter grade SCRs of 1200 V, 27 A ratings are used both in the rectifier as well as the CSI. The VSI is built using IGBTs of 1200 V, 75 A ratings with DC link capacitor of 2200 μF. Since the components available in the laboratory are used for building the experimental set-up the ratings of the devices mentioned above are much higher than the real requirements for a 3-HP synchronous motor drive. The CSI operation is at fundamental frequency while the VSI is operated at 1 kHz switching frequency. Hall effect based sensors are used for sensing the DC-link current (i_d) and the CSI line voltages (v_{sab} and v_{sbc}). The complete control scheme is implemented on a Digital Signal Processor TMS320F28335. Experimental results are shown from in Figures from 4.7 to 4.12. Figure 4.7 shows the motor voltage, the motor current, the DC-link current and the VSI capacitor voltage during the low speed operation of the motor at 30 RPM, which is 2% percent of the rated speed. Further, low speed operations of the motor till 10% of the rated speed are depicted in figures from Figure 4.8 to Figure 4.10. Figure 4.11 shows the motor operation at 300 RPM. Figure 4.12 shows motor acceleration from stand-still condition to 300 RPM. It can be observed that

the proposed scheme facilitates normal load commutation from starting of the motor, even in the absence of motor back-EMF. It can be seen that the voltage across the capacitor of the VSI is constant even during the acceleration. Figure 4.13 shows the photograph of the experimental setup.

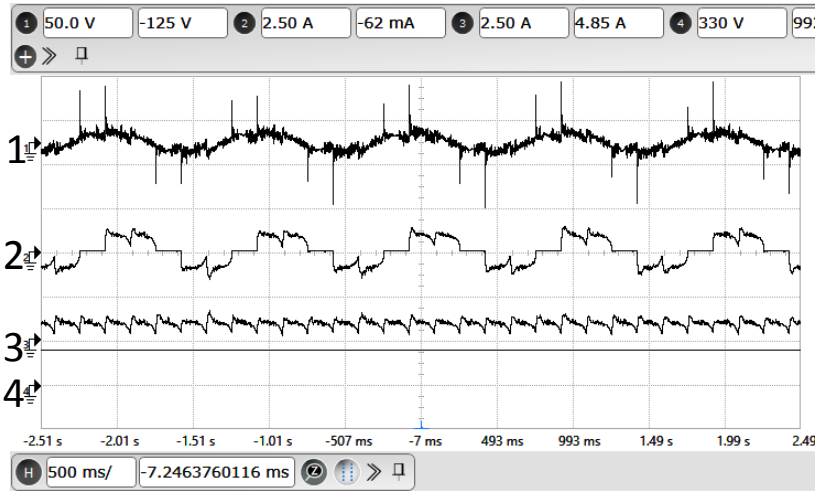

Figure 4.7: Experimental result at 30 RPM of motor operation: X-axis: 500 ms/div. Ch:1. Motor voltage (Y-axis: 50 V/div.). Ch:2. Motor current (Y-axis: 2.5 A/div.). Ch:3. DC-link current (Y-axis: 2.5 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 330 V/div.).

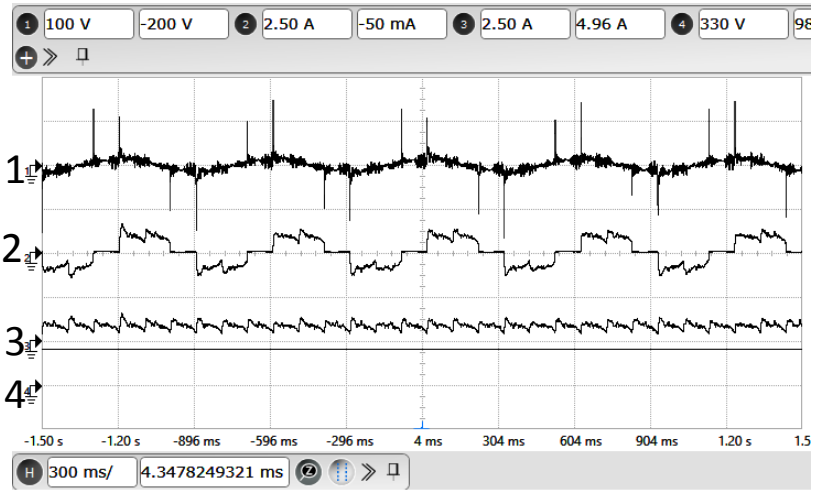

Figure 4.8: Experimental result at 50 RPM of motor operation: X-axis: 300 ms/div. Ch:1. Motor voltage (Y-axis: 100 V/div.). Ch:2. Motor current (Y-axis: 2.5 A/div.). Ch:3. DC-link current (Y-axis: 2.5 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 330 V/div.).

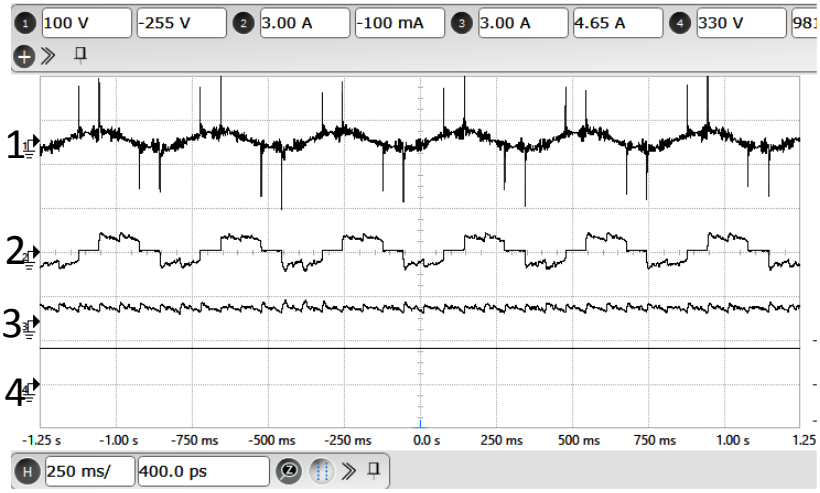

Figure 4.9: Experimental result at 75 RPM of motor operation: X-axis: 250 ms/div. Ch:1. Motor voltage (Y-axis: 100 V/div.). Ch:2. Motor current (Y-axis: 3 A/div.). Ch:3. DC-link current (Y-axis: 3 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 330 V/div.).

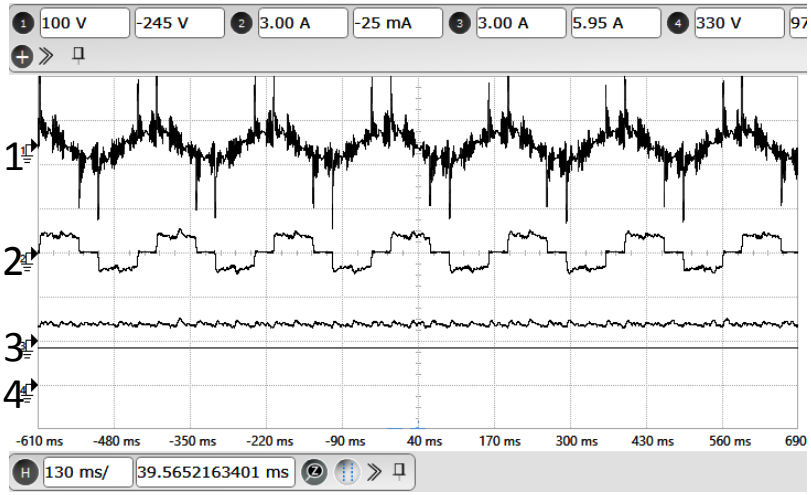

Figure 4.10: Experimental result at 150 RPM of motor operation: X-axis: 130 ms/div. Ch:1. Motor voltage (Y-axis: 100 V/div.). Ch:2. Motor current (Y-axis: 3 A/div.). Ch:3. DC-link current (Y-axis: 3 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 330 V/div.).

4.5 Conclusion

A new scheme for current source inverter (CSI) fed synchronous motor drive that ensures load commutation at start-up as well as low speed operation is presented in this chapter. This scheme is an attractive solution for the commutation failure at low speeds and torque pulsation due to pulsed mode operation encountered by the conventional SCR based CSI fed synchronous motor drives. The proposed drive consists of a synchronous motor with open-end stator windings fed by a CSI at one side of the windings while the other side is

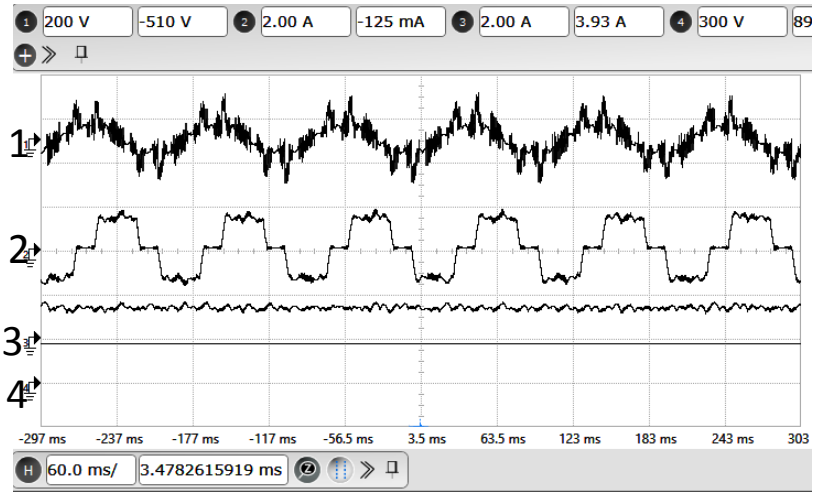

Figure 4.11: Experimental result at 300 RPM of motor operation: X-axis: 60 ms/div. Ch:1. Motor voltage (Y-axis: 200 V/div.). Ch:2. Motor current (Y-axis: 2 A/div.). Ch:3. DC-link current (Y-axis: 2 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 300 V/div.).

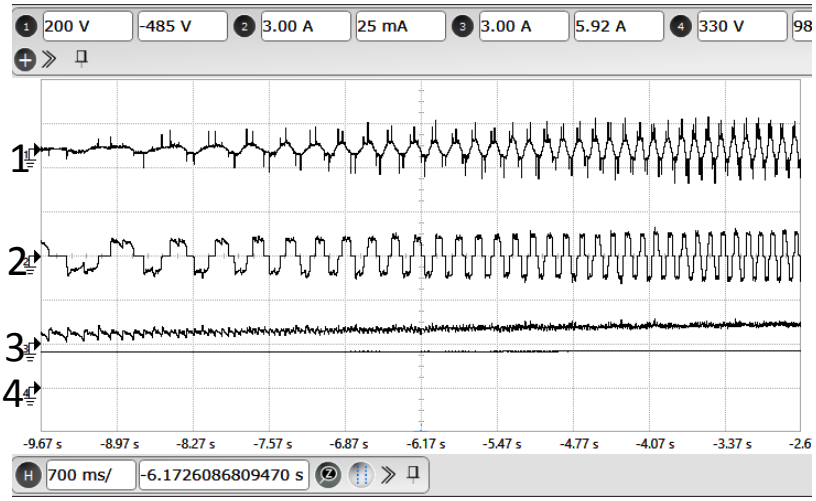

Figure 4.12: Experimental result for acceleration of motor from standstill state to 300 RPM: X-axis: 700 ms/div. Ch:1. Motor voltage (Y-axis: 200 V/div.). Ch:2. Motor current (Y-axis: 3 A/div.). Ch:3. DC-link current (Y-axis: 3 A/div.).Ch:4. VSI capacitor voltage (Y-axis: 330 V/div.).

connected to a capacitor fed voltage source inverter (VSI). The VSI will be in operation to facilitate load commutation only during start-up and low speeds. If the drive is required to be operated only in one quadrant and at high speeds the VSI can be disconnected from the system once the speed exceeds the change-over speed by using electrical contactors or turning ON all the upper (or lower) switches of the VSI. Alternatively, if four quadrant operation or frequent operation at low speeds without any interruption is required the VSI can be kept connected in the system. The VSI will inject a voltage in series with the

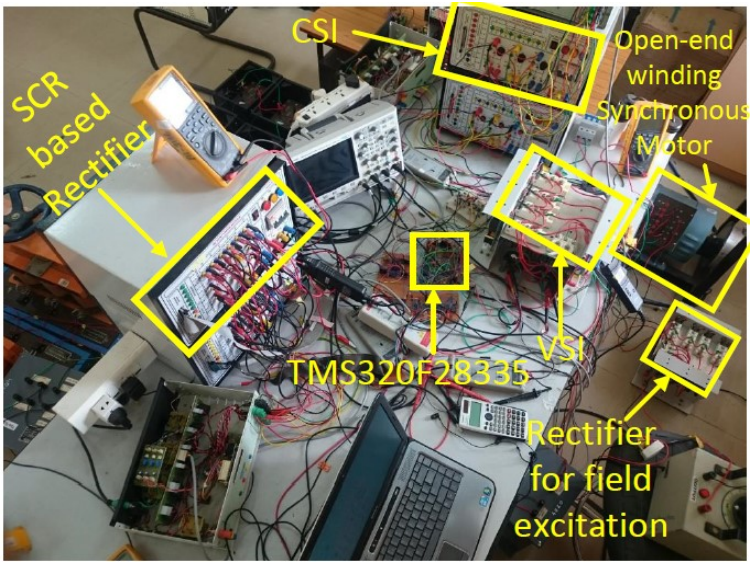

Figure 4.13: Photograph of the experimental setup

motor voltage whenever the back-EMF of the motor is not sufficient to commutate the SCRs. In the proposed drive the CSI is used for pre-charging the capacitor of the VSI and hence a separate pre-charging circuit is not required. Moreover, since the CSI remains to be the source of real power fed to the system, the drive has the capability to provide high starting torque which would be a requirement in many high power applications. This drive is capable of operating in all the four quadrants with easy and uninterrupted reversal of direction and regeneration. The proposed scheme is experimentally verified on a laboratory prototype under transient as well as steady state operating conditions. It is an attractive solution for the problem being faced by the industry in the field of synchronous motor drives.

Chapter 5

Hardware Organization

5.1 Introduction

In this chapter, details of the laboratory prototypes built for experimental verification of the proposed schemes for load commutated current source inverter fed drives are presented. The hardware setup mainly consists of the power circuit comprising of the SCR based rectifier, SCR based CSI, filter inductor, induction / synchronous motor and IGBT based VSI. Other supporting subsystems include SCR gate driver cards, IGBT gate driver cards, signal conditioning circuits, digital cards for SCR gating pulse train generation, voltage sensor card, current sensor card and the Digital Signal Processor (DSP)-TMS320F28335 used for implementing the control algorithm.

5.2 Power circuit

In the previous chapters the following three topologies were discussed in detail:

- Load Commutated SCR based CSI fed induction motor with open-end stator windings.
- Load commutated SCR based multilevel CSI fed induction motor with open-end stator windings.
- A series voltage compensated synchronous motor drive with load commutation at starting and low speed operation.

In all the above schemes the basic power circuit consists of SCR-based rectifier, filter inductor, SCR based CSI, and IGBT based capacitor fed VSI.

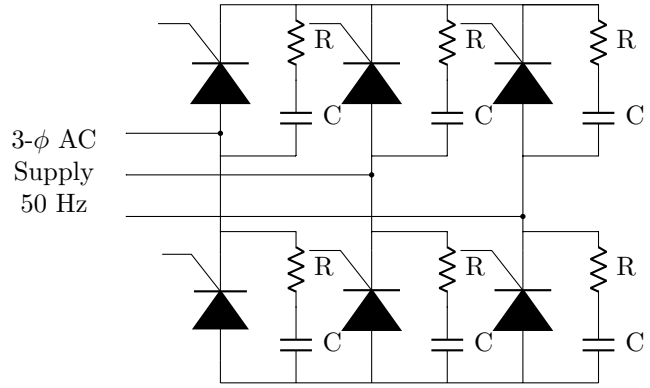

Figure 5.1: Power circuit diagram of SCR based rectifier.

5.2.1 SCR Based Rectifier

The controlled rectifier module is built using converter grade SCRs. Figure 5.1 shows the rectifier power circuit which consists of six SCRs rated at 1200V and 27A, with RC snubber circuit for protection. All the six SCR modules are placed on a common heat sink (air cooled). 'Semikron' make (model no: SKKT-27) SCR modules are used in the rectifiers. The SCR based rectifier along with an inductor of 200mH is used for building the current source.

5.2.2 Load commutated SCR based Current Source Inverter

Figure 5.2 shows the power circuit of load commutated SCR based current source inverter (CSI). The inverter is built using 'Semikron' make converter grade SCRs (model no: SKKT27B) of 1200 V and 27A ratings. Each SCR has a separate RC snubber circuit for protection and the complete SCR module is mounted on a common heat sink for proper cooling.

5.2.3 SCR gate driver card

The SCR modules of the rectifier and the CSI are triggered using pulse transformer based gate drive cards. The gate driver card unit consists of six isolated pulse transformers to trigger the SCRs into conduction. The basic gate driver circuit structure for SCR triggering is shown in Figure 5.3. The GPIO pins of the DSP are used to generate square

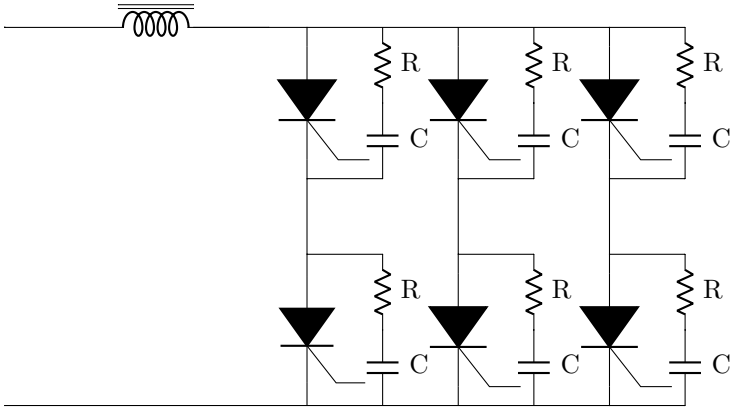

Figure 5.2: Power circuit diagram of Load commutated SCR based CSI.

wave pulses which are further converted into pulse trains by a digital gate driver card module for driving the transistor in the gate driver circuit (Figure 5.3). The frequency of the pulse train is 15kHz with 50% duty cycle. 50% duty cycle is maintained to provide sufficient time for flux reset of the pulse transformer to avoid magnetic saturation. The free wheeling diode at the primary side will reset the flux.

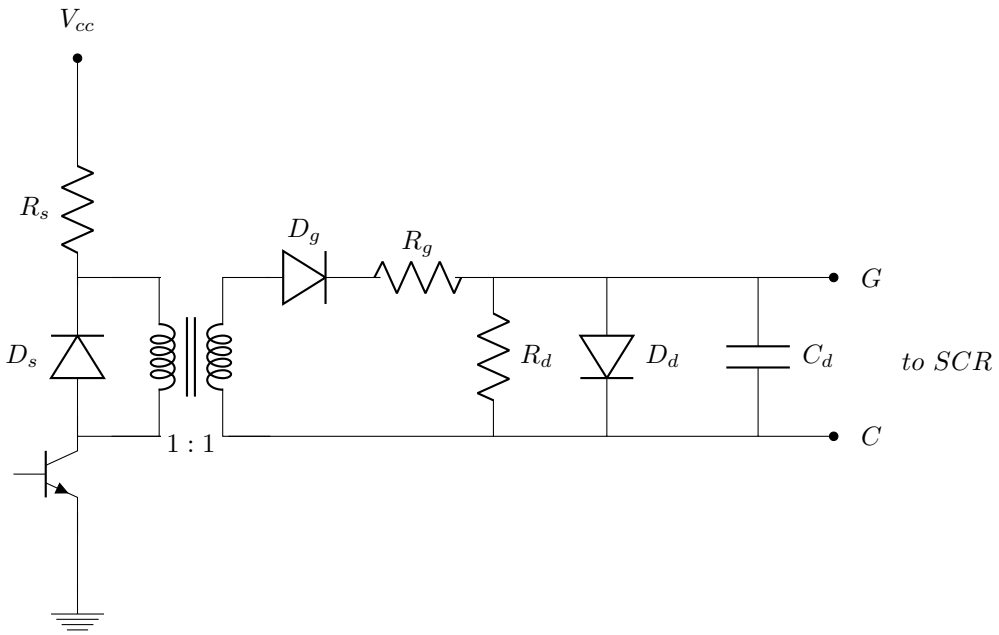

Figure 5.3: Circuit schematic of SCR gate driver.

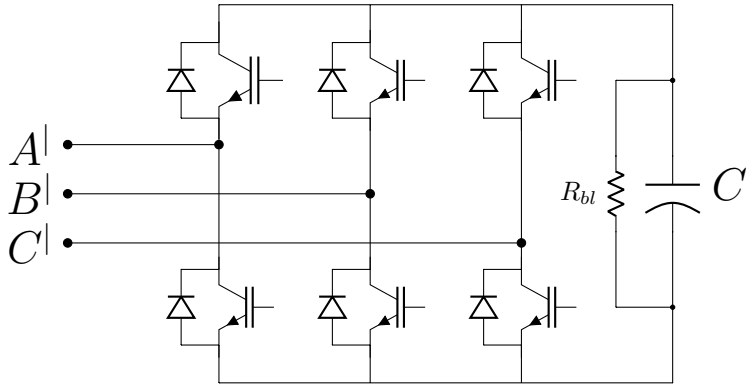

Figure 5.4: Power circuit diagram of IGBT based VSI.

5.2.4 IGBT based VSI (two-level VSI)

A three phase two-level voltage source inverter (VSI) is built using six insulated gate bipolar transistors (IGBT) and a DC link capacitor 'C' as shown in Figure 5.4. 'Semikron' make, 1200 V, 75 A IGBTs (model no: SKM75GB12T4) are used for building the VSI. The maximum operating frequency of this IGBT is 20 kHz. They are mounted on a heat sink (air cooled) for proper heat dissipation. The DC link capacitor is of electrolytic type (ALCON make), 2200 μF, 450 V rating, with a discharging resistor (R_{bl}) of 50 kΩ.

5.2.5 Gate driver card for IGBTs

The block diagram of the gate driver card used for triggering IGBT modules of VSI is shown in Figure 5.5. The driving pulses are generated by the EPWM modules of the DSP. A CPLD is used for preventing simultaneous turn ON of top and bottom IGBTs in an inverter leg. This CPLD disables the gating pulses fed to the IGBT gate driver IC if the driving pulses from the DSP are high simultaneously for both bottom and top IGBTs in a inverter leg, for any reason. A Darlington transistor pair array is used for current amplification before feeding the driving signals to the gate driver IC. 'Toshiba' make hybrid integrated IGBT gate driver IC M57962L is used to generate gating pulses for IGBTs. This IC provides optical isolation between the input and the output. It also has a de-saturation detector based short circuit protection system which will shut down the gating signals to the IGBTs in case a short-circuit fault occurs. The gate driver card also has isolated DC-DC converter modules to provide gating voltage levels of +15V and

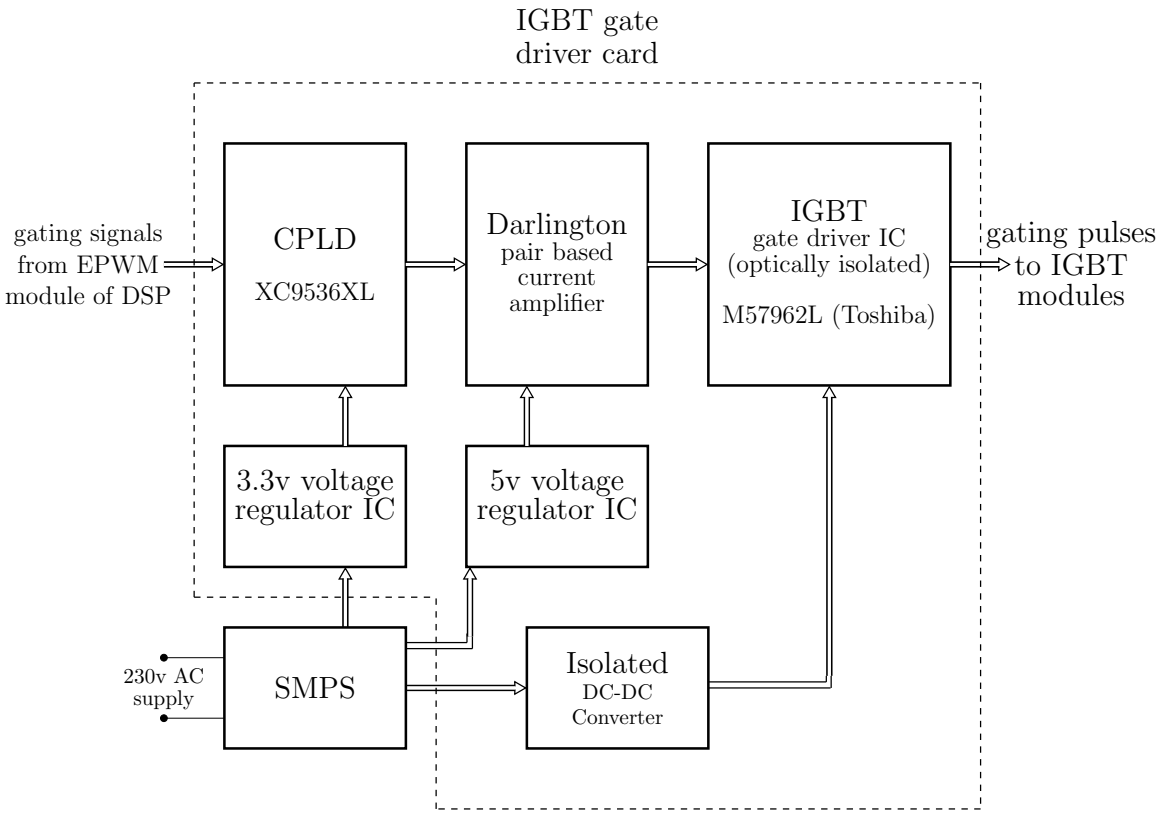

Figure 5.5: Block diagram of IGBT gate driver circuit.

-9V required for proper turn ON and turn OFF of IGBTs respectively. Regulated voltages of 3.3V and 5V required for CPLD and the current amplifier are also generated in the card using DC-DC converters.

5.3 Digital Signal Processor (DSP) and signal conditioning circuits

5.3.1 Digital Signal Processor

The control algorithms of all the schemes proposed in this thesis are implemented on a Texas Instruments make TMS320F28335 high performance Digital Signal Processor. It is a 32bit controller with an operating frequency of 150MHz and uses the clock generated by a crystal oscillator. There are various on-chip peripheral modules like analog to digital converter (ADC), enhanced Quadrature Encoder (eQEP) module, enhanced Pulse

Width Modulation (ePWM) module, General Purpose Input Output (GPIO) ports, Serial Communication Interface (SCI) and SPI. Figure 5.6 shows the block diagram of the DSP along with the on-chip peripherals and other added peripherals. 'Code Composer Studio'(CCS) software along with JTAG controller (XDS 100v2) is used for interfacing the DSP with computer for programming using C language. The bipolar ADC unit in the DSP board is used for capturing the analog signals like the voltage and current sensor outputs. Signal conditioning and level shifting circuits are used when bipolar signals have to be fed into uni-polar ADCs. Low pass filter having cut off frequency of 1.12 kHz is used for noise filtering. Figure 5.7 shows the Sallen-Key filter and the level shifting circuit. The bipolar AC signals are level-shifted by a DC voltage of 2.5V and attenuated by a factor of 4 thereby extending the effective range of the bipolar ADC unit as +6.3 V to -6.3 V. The input voltage range of the uni-polar ADC unit is 0 to +3 V. The output of the rotary incremental encoder fitted on the motor is fed to the on-chip Quadrature Encoder (eQEP) module of the DSP for measurement of the motor speed. The on-chip enhanced Pulse Width Modulation (ePWM) module is used for generating the gating pulses for the IGBTs. The dead-band required for IGBTs of an inverter leg can be programmed in the ePWM module. The general purpose input-output (GPIO) modules of the DSP are used for providing the gating pulses for the SCRs. A high precision 8-bit parallel uni-polar digital to analog converter (DAC) is used for signal monitoring and debugging.

5.3.2 Digital Card for SCR gating pulse train generation

The output gating pulses of the GPIO modules of DSP for SCR triggering is in the form of square wave pulses. Hence, a separate digital card for pulse train generation is built for converting the square pulses generated by the DSP into pulse trains for feeding to the SCR gate driver card. Figure 5.8 shows the block diagram of the pulse train generation card which basically consists of logic AND gates. The pulse train has a frequency of 15 kHz with 50% duty cycle.

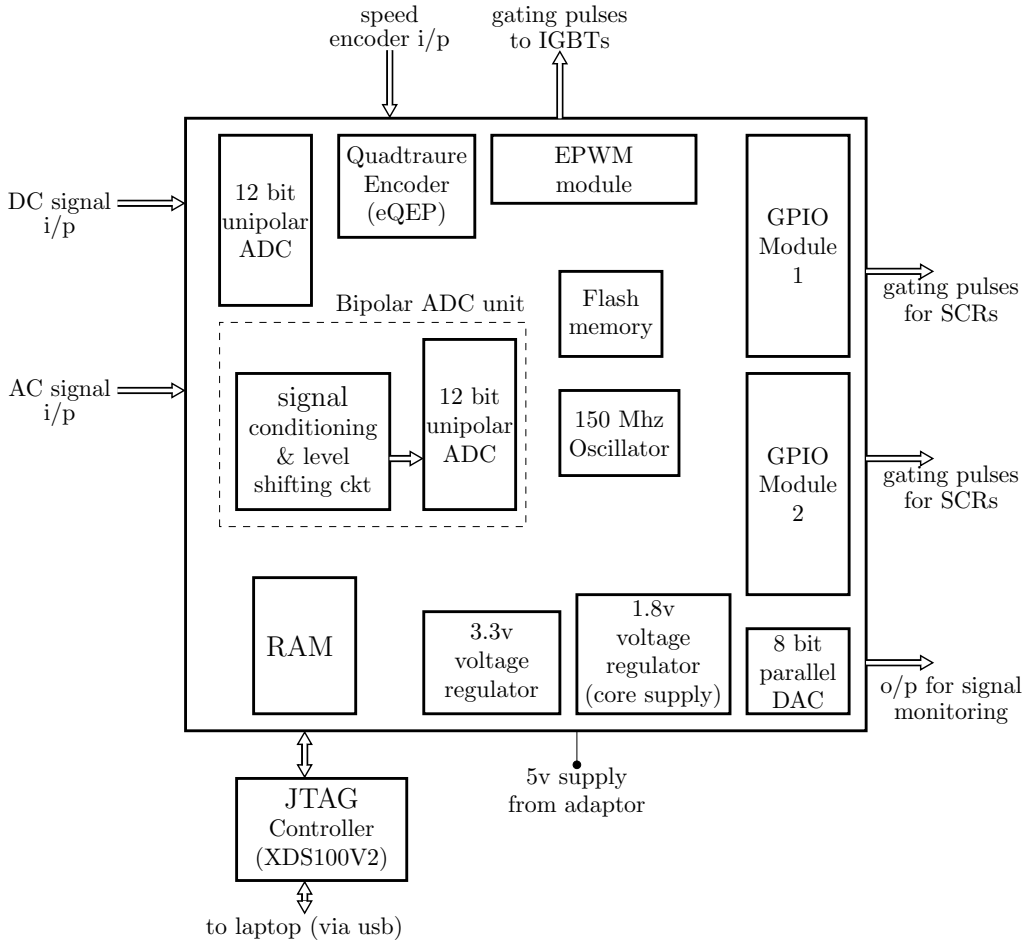

Figure 5.6: Block diagram of DSP board.

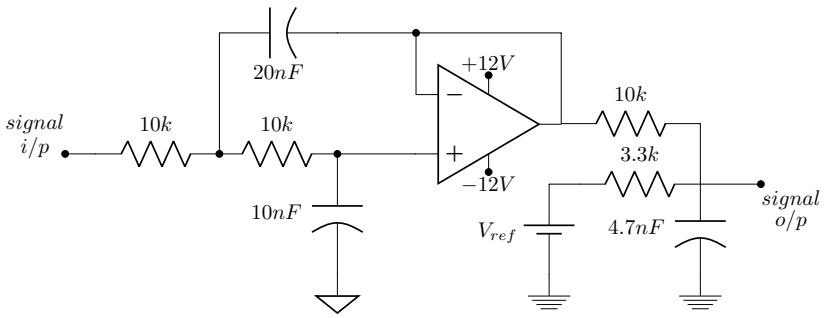

Figure 5.7: Circuit schematic of Sallen-Key filter.

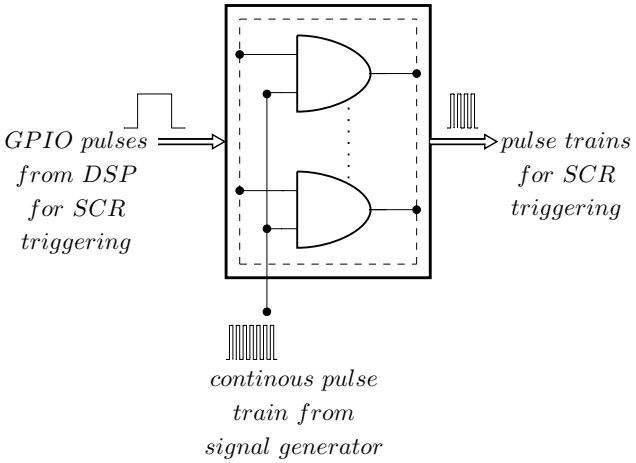

Figure 5.8: Block diagram of digital card for SCR gate pulse train generation.

5.3.3 Voltage sensor card

Voltage sensing is done using Hall effect based LEM voltage sensor, model no LV-20P. It can measure DC, AC and pulsed voltages with maximum range of 500 V and provides good galvanic isolation between the primary circuit (high voltage) and the secondary circuit (connected to DSP through ADC).

5.3.4 Current sensor card

Hall effect based current transducer, LEM make, model no:LV-55P is used for sensing currents. It can measure DC, AC and pulsed currents and provide galvanic isolation between the primary circuit (power circuit) and the low voltage devices in the secondary side (like the ADC of DSP board). The sensor requires dual power supply of +/-15 V which is provided to the sensor card externally. It can measure a current of 50 A (RMS) and a peak current of +/-75 A with an accuracy of +/-0.65%. A trim-pot is added to the sensor card to adjust the gain.

Chapter 6

Conclusions and Scope for Further Research

6.1 Summary of the research work

Load commutated current source inverter fed drives are extensively used in high power, medium voltage applications because of their advantages like simple and rugged structure, proven capability of easy regenerative braking, and low cost. In addition, the current source inverter fed drives have inherent protection against over-current, a very important feature that enhances the reliability in industrial applications. Regenerative braking is an important aspect in high power drives since the stored mechanical energy in the inertia of the motor and the load, which is substantial in high power drives, can be converted back to electrical energy. Regenerative braking thus significantly improves the efficiency of high power drives. One of the most important advantages of the load commutated SCR based CSI fed drives is the easy regeneration capability without any additional hardware requirement. The commutation of SCRs can be easily achieved if the load power factor is leading. Since the synchronous motors can be operated at leading power factor by resorting to over-excitation they are suitable for SCR based CSI fed drives. Hence the conventional SCR based load commutated CSI fed synchronous motor drives are very popular in the industry especially in high power applications.

Compared to the synchronous motors the induction motors are simpler, cheaper, very rugged and almost maintenance free and hence preferred in many industrial applications. However the induction motors are not amenable for operation as load commutated SCR based current source inverter fed drives as they always operate at lagging power factor.

Induction motor drive with parallel AC power capacitors at the motor terminals was one of the schemes tried for achieving load commutation, initially. A major drawback of this scheme was the resonance between the parallel capacitor bank and the motor inductance, in addition to commutation failure at slow speeds due to the insufficient reactive

power compensation. Hence external commutation circuit is required for low speed operation and starting. Later many hybrid topologies comprising of SCR based CSI and VSI connected in parallel at the induction motor terminal were proposed. However most of these hybrid topologies require separate DC source for the VSI in addition to an interfacing reactor for connecting the VSI to the motor terminals making the system bulky and expensive. Some of the schemes without interfacing inductor reported in the literature used an uncontrolled diode bridge rectifier as DC source for both VSI and CSI along with a DC-DC converter for feeding a variable voltage to the CSI thereby making the system more complex. In addition since a diode bridge rectifier is used for AC to DC conversion regenerative capability of the drive system is lost. Some other hybrid schemes reported in the literature need specially designed induction motor with two sets of three-phase windings on the stator. In many of such schemes low power / low voltage VSI is used for starting the induction motor thereby seriously compromising the torque and the power output of the drives during starting.

This research work addressed the problems in the field of CSI fed induction motor drives cited above and proposed new schemes for realization of load commutated SCR based CSI fed induction motor drives with open-end stator windings. The proposed schemes can be implemented on any induction motor by accessing both ends of the stator windings which are normally accessible through the terminal box fitted on the frame in all medium and high power induction motors. The open-end stator winding configuration is commonly used in realization of multilevel VSI fed drives. This research work for the first time explored the open-end stator winding configuration for realization of load commutated current source inverter fed motor drives. A new scheme for realization of load commutated SCR based current source inverter fed induction motor drive with open-end stator winding is presented in Chapter 2 of this thesis. In this topology a SCR based CSI is connected at one end of the stator windings for feeding active power to the motor and a capacitor fed IGBT based VSI is connected at the end of the stator windings for supplying reactive power. Load commutation of the SCRs of the CSI is achieved by controlling the VSI in such a way that it over-compensates the reactive power required by the motor so that at the CSI terminals the current leads ahead of the voltage. This scheme does not require any interfacing inductor or separate DC source for the VSI and can be implemented

for any induction motor by accessing both ends of the stator windings. This topology is also free from problems like commutation failure at low speeds normally encountered in CSI fed high power drives. As the VSI supplies only reactive power its rating is only a fraction of the rating of the CSI. Since the CSI is used for supplying active power to the motor always this drive is capable of delivering the rated torque even at start-up. This drive system also facilitates easy regenerative braking without any additional hardware. The proposed scheme is experimentally verified on an induction motor with open end stator windings under transient as well as steady state operating conditions.

The motor current in the CSI fed IM drive proposed in Chapter-2 is a quasi-square wave with significant amount of fifth and seventh harmonics which can cause high torque pulsations. Multilevel current source inverters can significantly improve the quality of motor current to achieve reduction in torque pulsations. In addition, multilevel configuration can reduce the device current rating requirement and also improve the reliability of the system by bringing in redundancy. A new scheme for realization of a SCR based load commutated multilevel CSI configuration for an open-end winding induction motor is proposed in Chapter-3 of this thesis. It consists of a load commutated SCR based multilevel CSI connected to one end of the stator winding to meet the real power requirement of the system, while the other end of the stator winding is directly interfaced with a capacitor fed IGBT based VSI for reactive power compensation. The CSI in the proposed scheme can be used for driving the motor even during start-up as well as low speed operation. As a result this drive is also capable of delivering rated torque in the entire speed range. The VSI does not require a separate interfacing inductor thereby reducing the size, weight and cost of the system. The proposed scheme does not require a separate DC source for the VSI or a buck converter for the CSI. This will substantially reduce the hardware complexity, size, weight and cost of the system. The multilevel motor current waveform results in a significant reduction in 5^{th} and 7^{th} harmonics. This reduction in 5^{th} and 7^{th} harmonics will result in substantial reduction of 6^{th} harmonic torque pulsations. In the proposed scheme, even when the two CSIs are operating with a phase shift of 30 degrees, load commutations of SCRs in both CSIs are achieved using the VSI. A new motor current oriented synchronously revolving reference frame based closed loop control scheme was developed and implemented to achieve this task. Regenerative braking

of the drive during which power flows from the induction machine to the supply source is achieved with load commutation of the SCRs, even when the two CSIs operate with a phase shift. Regeneration in the proposed topology also involves coordinated control of the two rectifiers, two current source inverters and the VSI. The closed loop control scheme proposed ensures smooth transition from motoring mode to regeneration mode and vice-versa. The proposed multilevel CSI fed drive scheme is experimentally verified on an induction motor with open end stator windings under transient as well as steady state operating conditions including regeneration.

A major problem faced in the conventional load commutated current source inverter fed synchronous motor drive is the commutation failure during low speed operation due to insufficient back-EMF. The scheme adopted by the industry as a solution for this problem is to employ pulsed mode of operation during starting and at low speed. However, the pulsed mode of operation results in undesirable high torque pulsation. A new scheme to facilitate hassle-free load commutation of CSI fed synchronous motor drives during starting as well as at low speed without resorting to pulsed mode operation is proposed in Chapter-4 of this thesis. The proposed scheme consists of an open-end winding synchronous motor with a SCR based current source inverter connected to one side of the stator windings and an IGBT based voltage source inverter connected to the other side to aid commutation of the SCRs when the back-EMF is insufficient. The CSI provides the real power requirement of the system, while the VSI is controlled to generate sufficient voltage which gets added to the motor back-EMF to facilitate load commutation during start-up and low speed operation. When the drive speed exceeds the change-over speed the VSI operation can be stopped and the CSI alone will be in operation. This can be achieved by shorting the VSI-side ends of the stator windings either by using electro-mechanical contactors or by turning ON all the upper (or lower) switches of the VSI. Alternatively, the VSI operation can be continued in the entire speed range if frequent operation at low speed or reversal of speed is required. The proposed scheme is experimentally verified on a 3-HP synchronous motor drive under all operating conditions including operation at very low speed.

All the new CSI fed drives schemes proposed in this thesis are experimentally verified using a digital processor for implementation of the control schemes. The details of the

experimental set up are given in Chapter-5 of the thesis.

6.2 Scope for further research

In all the schemes of load commutated SCR based CSI fed open-end winding drives proposed in this thesis two-level VSIs are used as series compensators. However in medium voltage drives it would be better to use multilevel voltage source inverters instead of two-level inverters to improve the quality of the voltage injected to the motor at reduced switching frequency. Multilevel inverter will also mitigate the EMI issues.

Since the VSI is basically used only for commutation of the SCR, the possibility of switching the VSI only at the time of commutation can be explored. This will reduce the switching frequency and the associated switching loss. The control scheme needs to be modified accordingly.

Common mode voltages produced by the PWM inverters are one of the major concerns in high power drives as it results in mechanical failure of the motor. This will be a new area of research since in the proposed schemes both VSI and CSI are connected to the motor.

Appendix

Appendix A

A.1 Details of major power circuit components

A.1.1 Squirrel Cage Induction Motor

1.5 hP, 415 V, 50 Hz, 4-pole, 1415 rpm, 3-phase with open-end stator windings.

Table A.1
Induction Motor Parameters

Parameter	Value
No of poles (P)	4
Inertia (J)	0.01 $Kg.m^2$
Stator Resistance (R_s)	$8.89\ \Omega$
Rotor Resistance (R_r)	$5.51\ \Omega$
Stator inductance (L_s)	24.36 mH
Rotor inductance (L_r)	24.36 mH
Magnetising inductance (L_m)	450.46 mH

A.1.2 SCR based Rectifier

C20 MCB used at the input side of the rectifier.

Additionally each phase is placed with 10A fuse for fast over current protection.

Devices used: Three, thyristor modules SEMIPACK, SKKT-27B16E, I_{TAV}= 27A ($T_c = 82^oC$), I_{Trms}= 50A,V_{RRM},V_{DRM}=1200 V.

Device holding current (I_H) =200mA, latching current (I_L)= 400mA.

Minimum gate trigger voltage (V_{GT})= 3V.

Minimum gate trigger current (I_{GT})= 150mA.

Device turn off time (t_q)= 80μ s.

Proper heat sink, RC-snubber circuit for cooling and $\frac{dV}{dt}$ protection respectively.

Since the SCR gate pulses of the rectifier are to be synchronized with the line supply a

step down transformer of 0 to 15V is used to sense the supply voltage. This voltage is further steeped down and fed to DSP to generate the gating pulses.

A.1.3 Load commutated SCR based CSI

DC choke: Iron cored variable inductor fixed at 200mH, from Vi-microsystems. C20 MCB used at the input side of the inverter module.

Additionally each phase is placed with 10A fuse for fast over current protection.

Devices used: Three, thyristor modules SEMIPACK, SKKT-27B16E, I_{TAV}= 27A ($T_c = 82^0C$), I_{Trms}= 50A,V_{RRM},V_{DRM}=1200 V.

Device holding current (I_H) =200mA, latching current (I_L)= 400mA.

Minimum gate trigger voltage (V_{GT})= 3V.

Minimum gate trigger current (I_{GT})= 150mA.

Device turn off time (t_q)= 80μ s.

Proper heat sink, RC-snubber circuit for cooling and $\frac{dV}{dt}$ protection respectively.

A.1.4 SCR gate driver card

Six 1:1 pulse transformers from PULSE TEK used to trigger six SCRs.

Gate drive current: 230 mA

Gate voltage: Open circuit-5V.

A.1.5 IGBT based VSI

Device used: Three, Semikron IGBT modules SKM75GB12T4, V_{CES}=1200V, I_{Cnom}=75A.

DC bus capacitor: Single 2200uF, 450 V of ALCON make.

A.1.6 Current sensor card

LA 55-P-LEM-Current Transducer.

I_{PN}= 50 A

Frequency Bandwidth: DC to 200kHz.

A.1.7 Voltage sensor card

LV 20-P-LEM-Voltage Transducer.

I_{PN}=10mA

V_{PN}=10 to 500 V

A.2 Converter Rating

In the series voltage compensated load commutated synchronous motor drive proposed in this thesis, the voltage rating of the VSI is decided based on the voltage requirement to ensure successful commutation of the SCRs of the CSI when the back-EMF is insufficient for commutation at start-up and during low speed operation. As mentioned in Chapter-4, if the VSI can provide 10% of the rated voltage of the motor, the commutation of the SCRs can be ensured during starting and low speed operation. For a 1 MW, 6.6 kV (line voltage), synchronous motor drive, the rating of the converters required will be as follows.
Fundamental voltage of the VSI = 10% of 6.6 kV = 660 V (line voltage)
Line voltage of 660V from the VSI can be achieved with a DC bus voltage (capacitor voltage) of 1077 V assuming sinusoidal pulse width modulation scheme at a modulation index of 1. Assuming a device (IGBT) selection safety factor of 1.5, a standard 1.7 kV IGBT device can be used for the VSI.
The SCRs of the CSI have to be rated for the machine voltage level (ie. 6.6 kV). Assuming a device safety factor of 1.5, the voltage rating of the SCR should be 9.9 kV.
The current ratings of the SCRs in CSI and the IGBTs in VSI would be the same. In the example of 1 MW, 6.6 kV drive the current rating of the switching devices would be approximately 200 A, considering the factor of safety.

Single IGBTs of current rating up to 1800 A are now commercially available. Hence, single VSI would be sufficient to meet the current rating of the drive in the low power

range. However, in the high power range of LCI fed drives with current ratings above 900 A, parallel modules in the VSI would be necessary to meet the current rating (considering a factor of safety of 2).

A.3 Experimental verification on a 10 HP open-end winding induction motor

Additionally, the proposed load commutated SCR based current source inverter (both single CSI and multilevel CSI) fed induction motor drive with open-end stator windings is verified on a 10 HP, 415V, 50 Hz, 1450 rpm open-end winding IM with the help of digital signal processor TMS320F28335. Some of the experimental results are presented below,

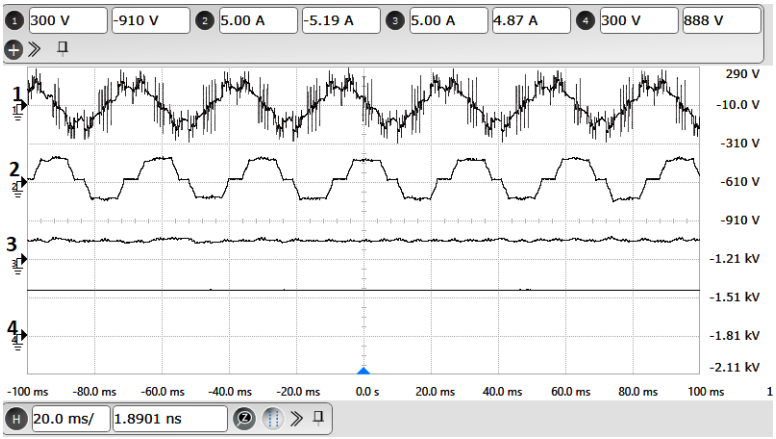

Figure A.1: Experimental results with single CSI configuration: Motor operation at 1000 RPM : X-axis: 20 ms/div. Ch-1: A-phase stator voltage (Y-axis: 300 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

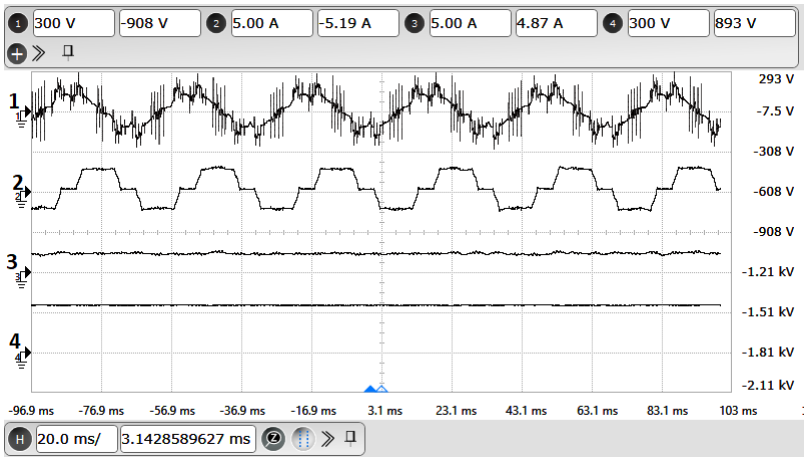

Figure A.2: Experimental results with single CSI configuration: Motor operation at 900 RPM : X-axis: 20 ms/div. Ch-1: A-phase stator voltage (Y-axis: 300 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

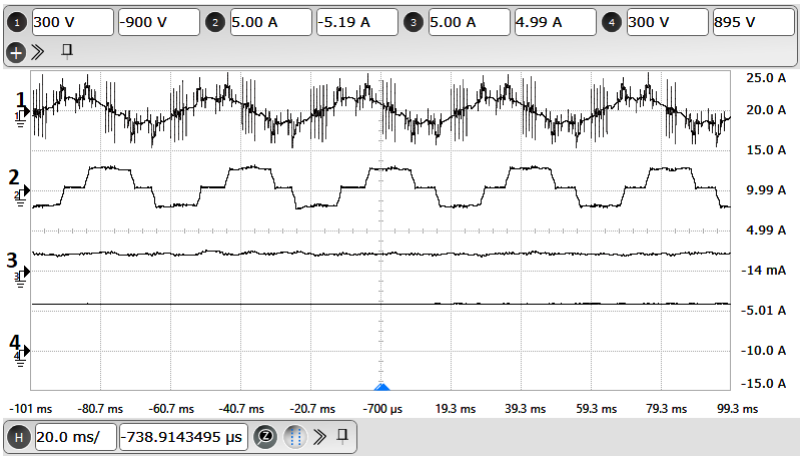

Figure A.3: Experimental results with single CSI configuration: Motor operation at 750 RPM : X-axis: 20 ms/div. Ch-1: A-phase stator voltage (Y-axis: 300 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

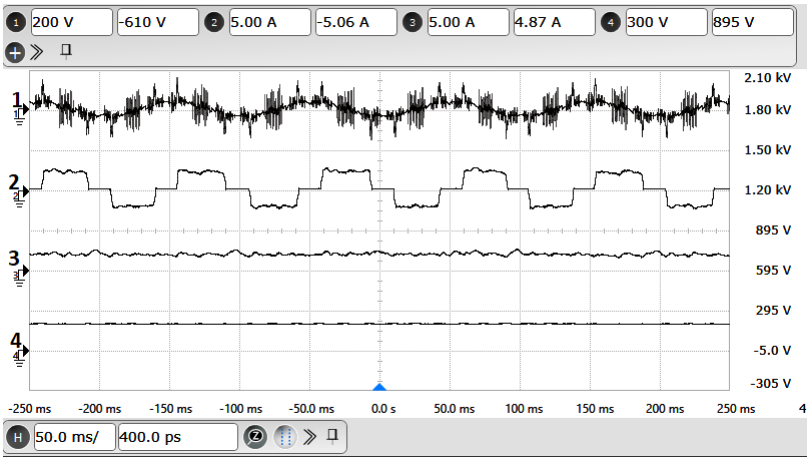

Figure A.4: Experimental results with single CSI configuration: Motor operation at 300 RPM : X-axis: 50 ms/div. Ch-1: A-phase stator voltage (Y-axis: 200 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

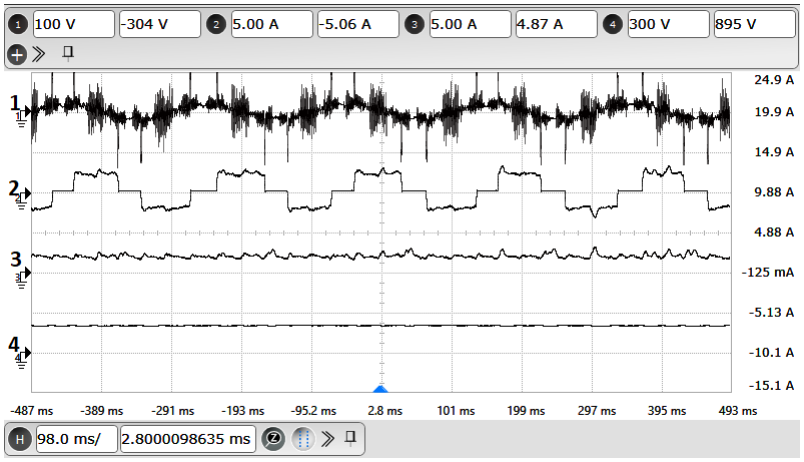

Figure A.5: Experimental results with single CSI configuration: Motor operation at 150 RPM : X-axis: 98 ms/div. Ch-1: A-phase stator voltage (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 300 V/div).

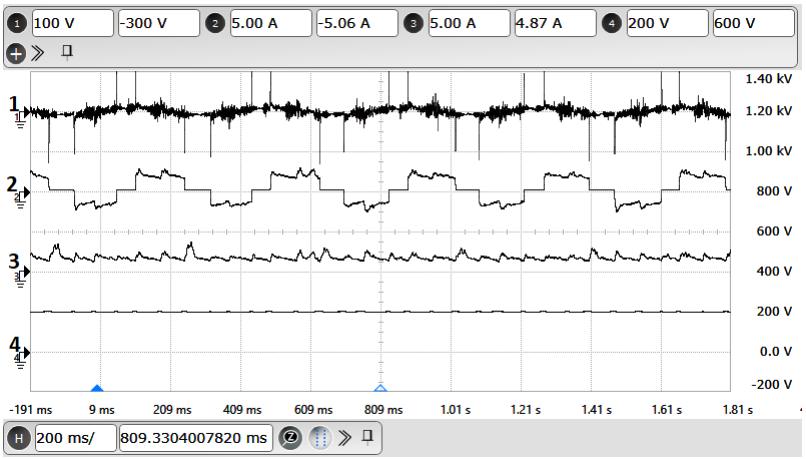

Figure A.6: Experimental results with single CSI configuration: Motor operation at 150 RPM : X-axis: 200 ms/div. Ch-1: A-phase stator voltage (Y-axis: 100 V/div). Ch-2: A-phase motor current (Y-axis: 5 A/div) . Ch-3: DC link current (Y-axis: 5 A/div) . Ch-4: VSI capacitor voltage (Y-axis: 200 V/div).

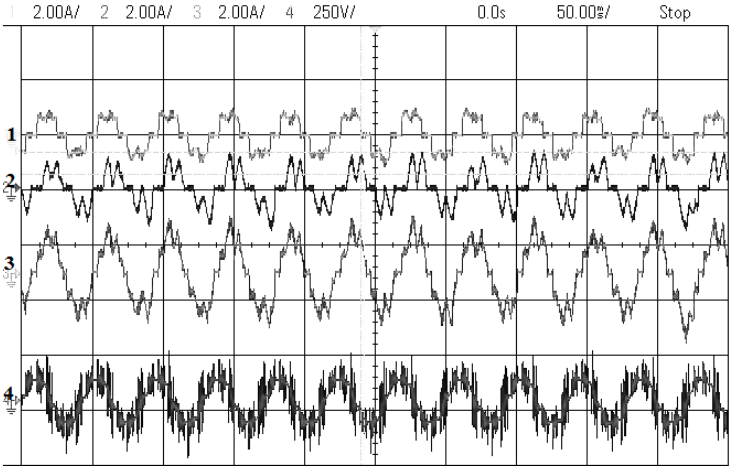

Figure A.7: Experimental results with multilevel CSI configuration : Motoring operation at 750 RPM: X-axis: 50ms/div. Ch-1: A-phase CSI-1 current (Y-axis: 2 A/div). Ch-2: A-phase CSI-2 current (Y-axis: 2 A/div) . Ch-3: A-phase motor current (Y-axis: 2 A/div). Ch-4: A-phase stator voltage of motor (Y-axis: 250 V/div).

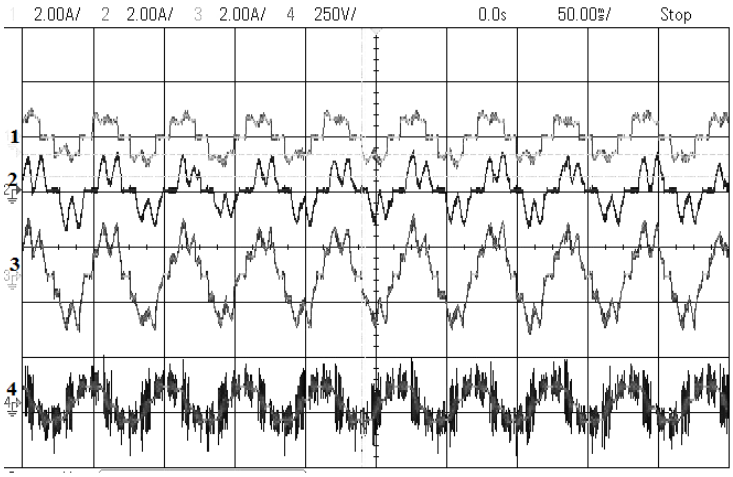

Figure A.8: Experimental results with multilevel CSI configuration : Motoring operation at 500 RPM: X-axis: 50ms/div. Ch-1: A-phase CSI-1 current (Y-axis: 2 A/div). Ch-2: A-phase CSI-2 current (Y-axis: 2 A/div) . Ch-3: A-phase motor current (Y-axis: 2 A/div). Ch-4: A-phase stator voltage of motor (Y-axis: 250 V/div).

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List of Publications

International Journal Papers

1. **Richu Sebastian C.** & Rajeevan P.P. Load-Commutated SCR-Based Current Source Inverter Fed Induction Motor Drive With Open-End Stator Windings. **IEEE Transactions on Industrial Electronics**, Vol.65, No.3, March 2018, 2031-2038.

2. **Richu Sebastian C.** & Rajeevan P.P. A Load Commutated Multilevel Current Source Inverter fed Open-end Winding Induction Motor Drive with Regeneration Capability. **IEEE Transactions on Power Electronics**, Vol.35, No.1, Jan 2020, 816-825.

3. **Richu Sebastian C.** & Rajeevan P.P. A Series Voltage Compensated Synchronous Motor Drive with Load Commutation during Starting and Low Speed Operation. **IEEE Journal of Emerging and Selected Topics in Power Electronics.**
(DOI:10.1109/JESTPE.2020.2966574)

International Conference Papers

1. **Richu Sebastian C.** & Rajeevan P.P. A new scheme for SCR based Current Source Inverter fed Induction Motor drive with open-end stator windings. *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, December 14-17, 2016.

2. **Richu Sebastian C.** & Rajeevan P.P. Load Commutated SCR Based Multilevel Current Source Inverter Fed Induction Motor Drive. *IEEE 27th International Symposium on Industrial Electronics (ISIE)* , Cairns, QLD, Australia, June 13-15, 2018.

3. **Richu Sebastian C.** & Rajeevan P.P. Four quadrant operation of load commutated SCR based multilevel CSI fed open-end winding Induction motor drive. *IEEE*

IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES) , IIT-Madras, Chennai, Dec 18-21, 2018.