A High Throughput Multi-scale Optical Flow Architecture And Its Application Towards Cloud Tracking

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Abstract

Optical flow (OF) computation for fast moving objects is an integral part of many vision systems. It uses an OF constraint to measure the relative displacement of all pixels between two consecutive frames of a video sequence. Most of the high-performing OF algorithms in the literature are based on variational OF algorithm proposed by Horn and Shunck (HS). HS formulates the OF computation as a global optimization problem which can be solved by iteratively minimizing the cost functional using a numerical solver. The OF constraint used as data term in the cost functional is valid only for capturing slow-moving objects. Hence the OF constraint is replaced by a non-linear image differencing constraint with a multi-scale or coarse to fine warping approach to compute large displacement. The large displacement OF computation finds a lot of application in high data rate applications ranging from vision aided robots to the near real-time analysis of atmospheric clouds. Realization of such a system requires high-speed computation of OF with deterministic latency and negligible accuracy loss.

The CPU implementation of variational multi-scale OF algorithm for high-resolution images in real-time is restricted due to the high data rate, the serial execution of pyramid levels, and the high memory bandwidth required for buffering and retrieving the image pyramids and the intermediate flow vectors. Hence this research work identifies the bottlenecks of the variational multi-scale OF algorithm and devises various architecture modification to enhance the throughput while reducing the resource utilization and power consumption. There are three challenges in the variational multi-scale OF algorithm, (1) the large number of arithmetic operations involved in the computation of every flow values, (2) the presence of various feedback loops corresponding to the number of pyramid levels, flow refinements and solver iterations, (3) the high memory bandwidth required for buffering and retrieving intermediate flow vectors and the huge amount of storage needed for buffering the image pyramids as well as the intermediate flow vectors.

These limitations are overcome by making various hardware adaptations to the variational multi-scale OF algorithm which involves the restriction of the complex and resource-intensive flow refinement loop to a single iteration without much loss in accuracy, utilizing a Jacobi solver whose current pixel value depends only on the neighbourhood pixels of the previous iteration instead of a Successive Over Relaxation (SOR) solver, eliminating

some of the complex repetitive arithmetic logic present in each solver iterations to a single arithmetic logic before the solver stage to reduce the resource utilization. The work proposes a variable fixed point time-sharing architecture for the modified algorithm and utilizes parallel architectures for solver, gradient, denoising and interpolation modules to improve the throughput while reducing the resource consumption. It also introduces three different memory banking schemes with customized access pattern for the pyramid, warping and flow resizing stage to improve the system throughput while minimizing the storage requirement. The proposed variational multi-scale OF architecture achieves a frame rate of 306 fps for High Definition (HD) image which is the highest when compared to the state of the art architectures. It makes use of 169 super-scalar units with 702 deep pipelines to achieve a throughput of 395 Giga Operations Per Second (GOPS) with a computation density of 21.5 GOPS/Watt on a Xilinx Virtex 7 device. The work also proposes various fixed and floating point hardware variants of the variational multi-scale OF algorithms to analyse the tradeoff in terms of area, power consumption and accuracy.

The variational multi-scale OF architecture is further analysed in terms of resource utilization and the flow accuracy, which leads to the design of the improved architecture for solver and flow filtering stage. The solver stage consumes the highest area in the proposed variational multi-scale OF architecture. So in order to reduce resource utilization of solver stage, different types of solvers are analysed to come up with a high throughput Red-Black Successive Over-Relaxation (RBSOR) solver architecture. The proposed RBSOR solver architecture is utilized for implementing a variational OF architecture. The proposed variational OF architecture is deeply pipelined to achieve high throughput and provides better accuracy at the cost of a lesser number of iteration compared to other solver implementations. It computes OF for Ultra High Definition (UHD) frames at 48 fps reaching a throughput of 406 Megapixels/s achieving a power efficiency of 43 Giga Operations Per Second/Watt (GOPS/Watt) on a Xilinx Virtex-7 device while operating at 412 MHz.

The flow denoising at each pyramid level of the variational multi-scale OF architecture with fewer solver iterations has a significant impact on the OF accuracy. Hence a more accurate and edge-preserving Bilateral Filter (BF) architecture is considered for flow denoising. But the large computational complexity and poor performance of the BF algorithm motivated to design a High Throughput Bilateral Filter (HTBF) architecture. The unfolding of the architecture utilizing the separability and symmetry property of the filter kernel is explored to reduce the computational complexity. The architecture utilizes a streaming variance compute module to dynamically adapt the range filter coefficients in accordance with the varying noise level. The proposed HTBF architecture can denoise UHD flow fields

at 53 fps on a Xilinx Virtex-7 FPGA device. The proposed fixed and floating point variants of the HTBF architecture achieves a power efficiency of 318 GOPS/W at 470 MHz and 37 Giga Floating-point Operations Per Second/Watt (GFLOPS/W) at 190 MHz respectively.

The proposed multi-scale architecture with improved RBSOR and HTBF subsystems is best suited for embedded vision applications, but the current work focuses on the design of a hardware accelerator for cloud/cyclone tracking and analysis based on a selective choice of various computer vision algorithms and the aforementioned architectures. It aids in taking necessary precaution against extreme climatic effects, helps to study the cloud system interactions using near-real-time satellite data. The software implementation of the proposed cloud analysis framework is computationally intensive and requires large processing time. This motivated to the design of a hardware architecture for cloud accelerator achieving a throughput of 71 fps for HD frames on Xilinx Virtex UltraScale+ device interfaced to host PC via Peripheral Component Interconnect Express (PCIe).