Methods for eliminating the limit cycle oscillation due to low resolution ADC/DPWM in digitally controlled DC-DC converters

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by

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ABSTRACT

Digital controllers have become an attractive choice in DC-DC converter as they have a number of potential advantages which include lower sensitivity to parameter variations, programmability, improvement in dynamic response by incorporating advanced control algorithm, auto tuning and communication capability. Most of the digital controllers are based on conventional architectures where Analog to Digital Converters (ADC) are used to digitize the converter state variables. A digital control algorithm estimates the duty cycle, which is given to a Digital Pulse Width Modulator (DPWM) to generate the Pulse Width Modulated (PWM) waveform. To achieve better regulation of the output voltage, a high speed and high resolution ADC is required to sample the output voltage at PWM switching frequency. Furthermore, the resolution of DPWM should be greater than that of the ADC to avoid undesirable quantization effects such as limit cycle oscillation. The design platforms for the digital controller are FPGAs, ASICs and DSP Processors. But there are practical limitations to the implementation of a power and area efficient ASIC. Hence, different methods to realize high speed, high resolution ADC and DPWM have been reported. But all the earlier reported work has its own drawback. However, no detailed studies are reported that implements a digital controller with low resolution ADC and DPWM as it may lead to limit cycle oscillation.

In the thesis, investigation was carried out to reduce the limit cycle oscillation due to low resolution ADC and DPWM. Thus the thesis primarily focuses on a reduced state, computationally efficient Kalman filter for reducing the limit cycle oscillation due to low resolution ADC. The thesis also focuses on a scheme to use low resolution DPWM with no limit cycle oscillation. Significant attempts were made to improve the conducted emissions from the converter, apart from improving the effective resolution.

The contribution of the thesis is summarized as given below.

I) A reduced state Kalman filter is proposed to reduce the limit cycle oscillations caused by low resolution ADCs in digitally controlled DC-

DC converter. The reduction in state of the converter has facilitated the minimization of the clock cycle required for computation. This has been achieved by reducing the vector states of converter to scalar state with Kalman gain computed offline.

II) A novel method for the reduction in limit cycle oscillation due to low resolution DPWM by combining the advantages of sigma delta modulation scheme and frequency modulation of switching frequency has been proposed. In this work, the correction of quantization error due to low resolution DPWM is accomplished by changing the switching frequency. The error due to the quantization of DPWM is accumulated for few clock cycles and the switching frequency is adjusted in the last cycle such that the duty ratio changes by the number of LSBs corresponding to the quantization error. The quantization error correction increases the effective resolution of DPWM thereby reducing the ripple due to limit cycle oscillations. Further, it also reduces the conducted electromagnetic emissions.

III) A most appropriate design for the digital controller by using low resolution ADC (6-bit) and DPWM (7-bit) by combining the reduced state Kalman filter and quantization error correction has been proposed. The reduced state Kalman filter gives the optimal output voltage from the noisy measurement from low resolution ADC and the quantization error correction increases the effective resolution of DPWM.